

Sheet: DC_IN
File: VNA_1.sch

Sheet: CLK Generation
File: CLK_Generation.sch

Sheet: Source
File: Source.sch

Sheet: Source-ATT-AMP
File: VNA_4.sch

Sheet: 1. LO
File: 1_LO.sch

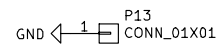
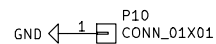
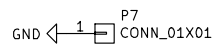
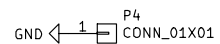
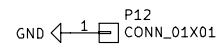
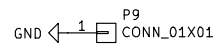
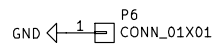
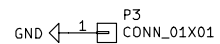
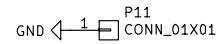
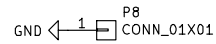
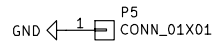
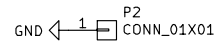
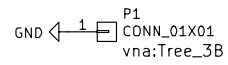
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Sheet: Port 2-MIX
File: Port_2.sch

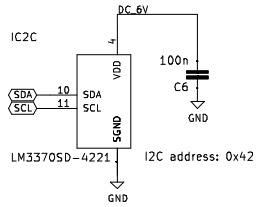
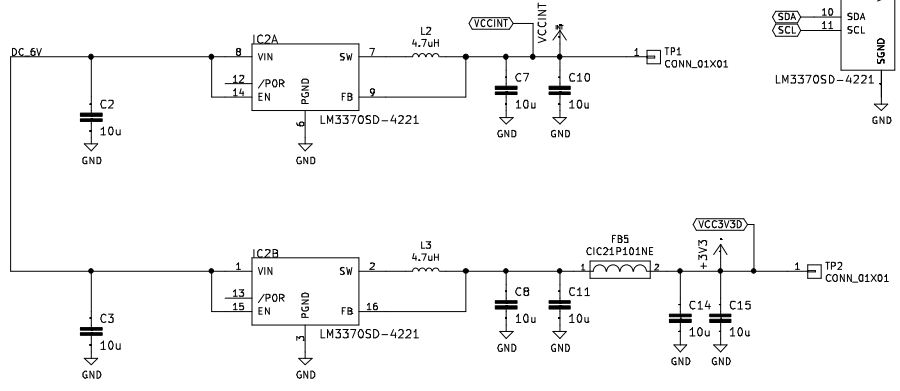
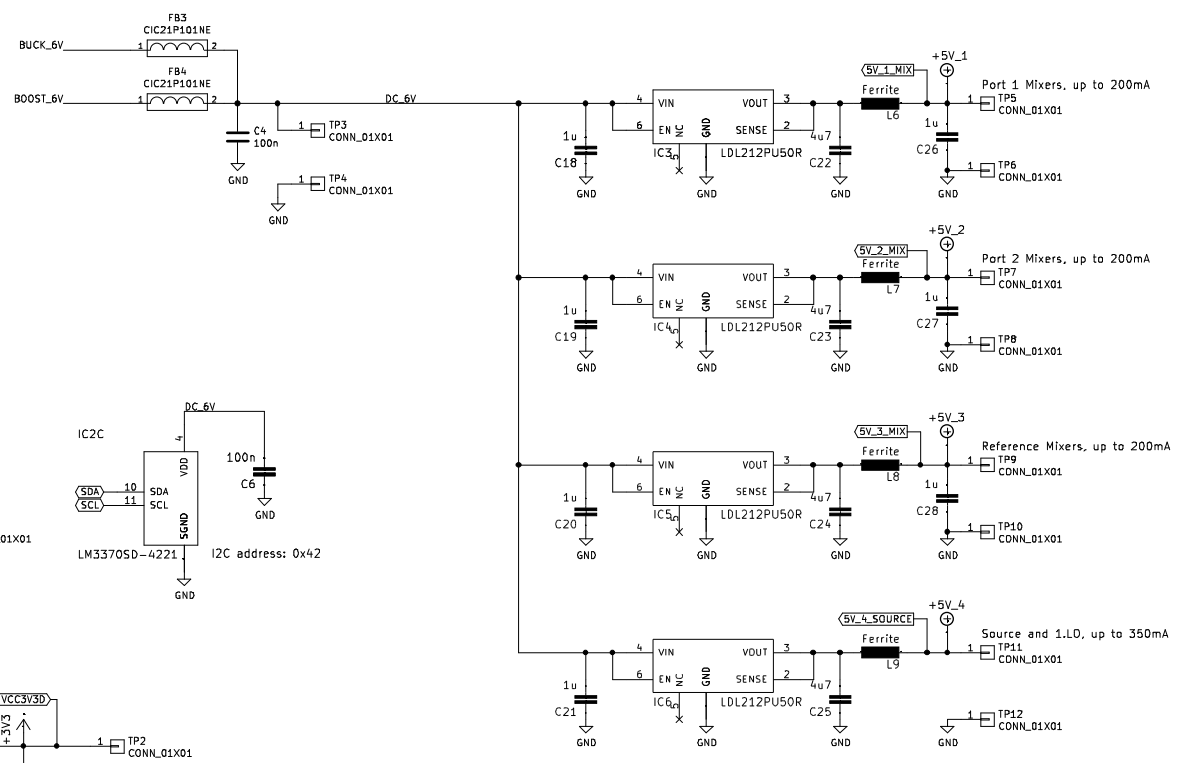
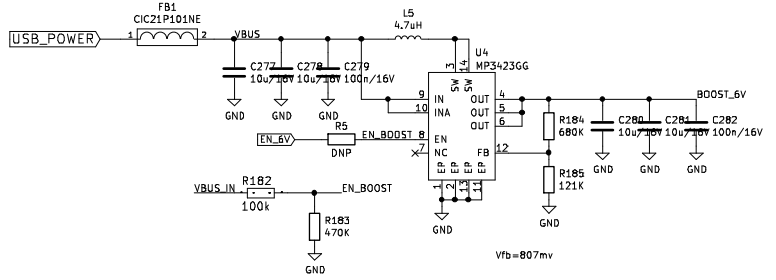
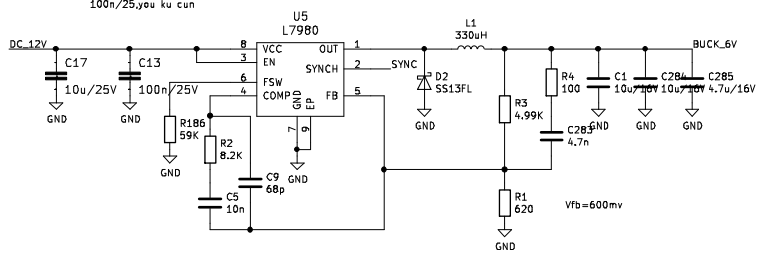
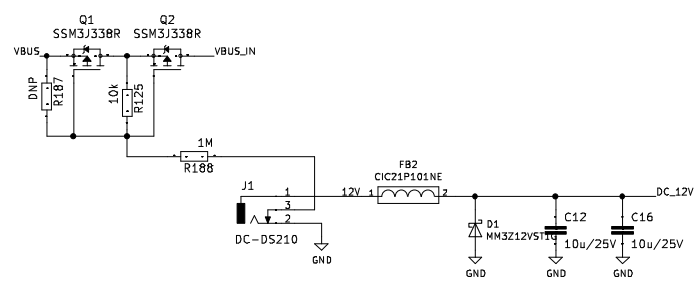
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Sheet: STM32
File: VNA_9.sch

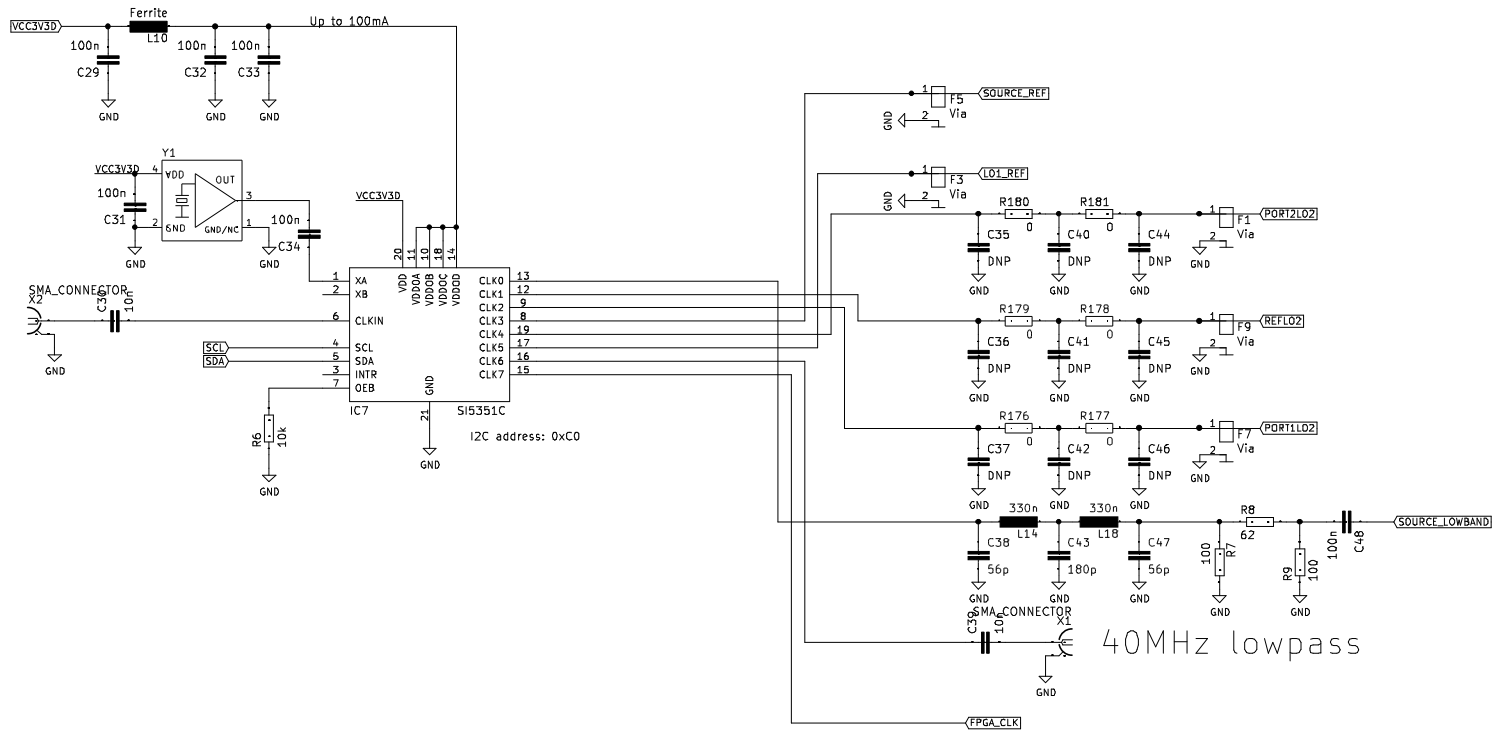
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File: VNA_10.sch



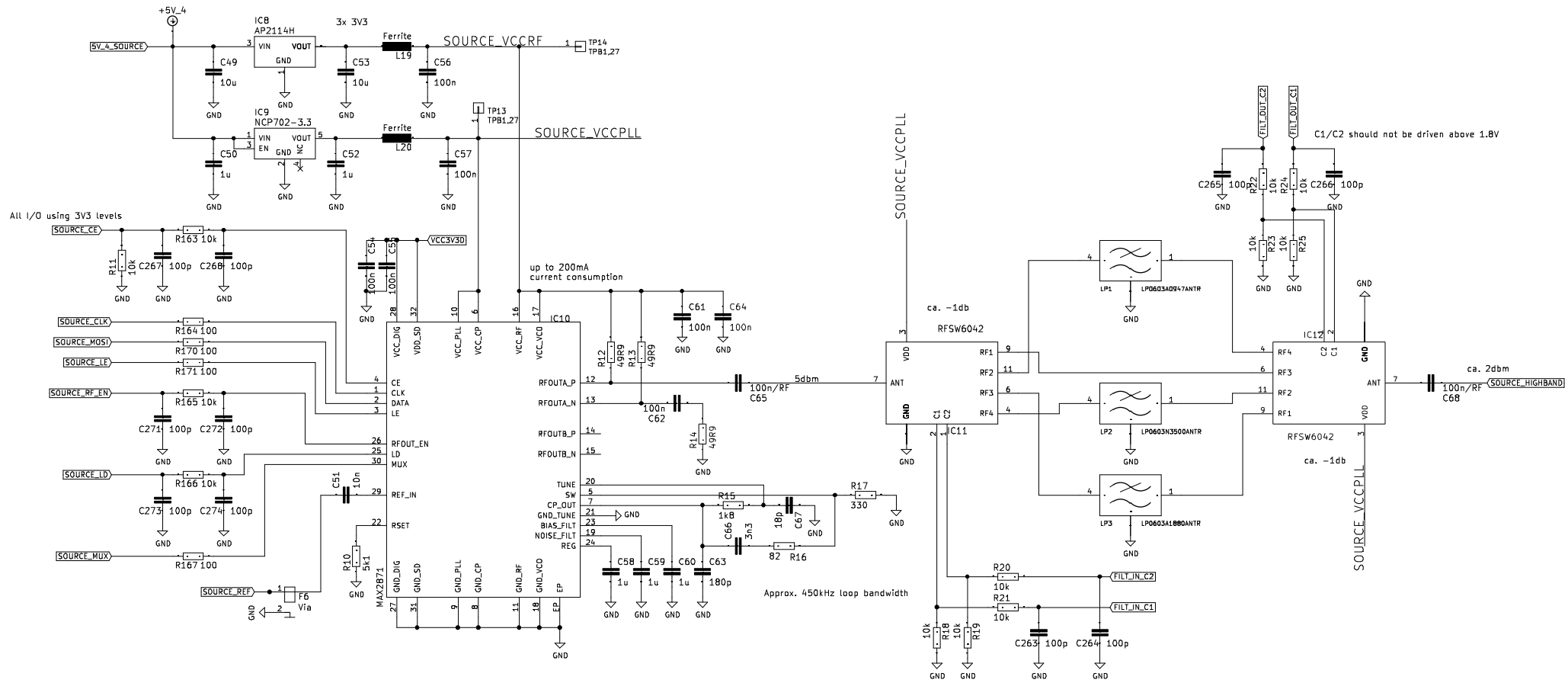
100n/25jou ku cun



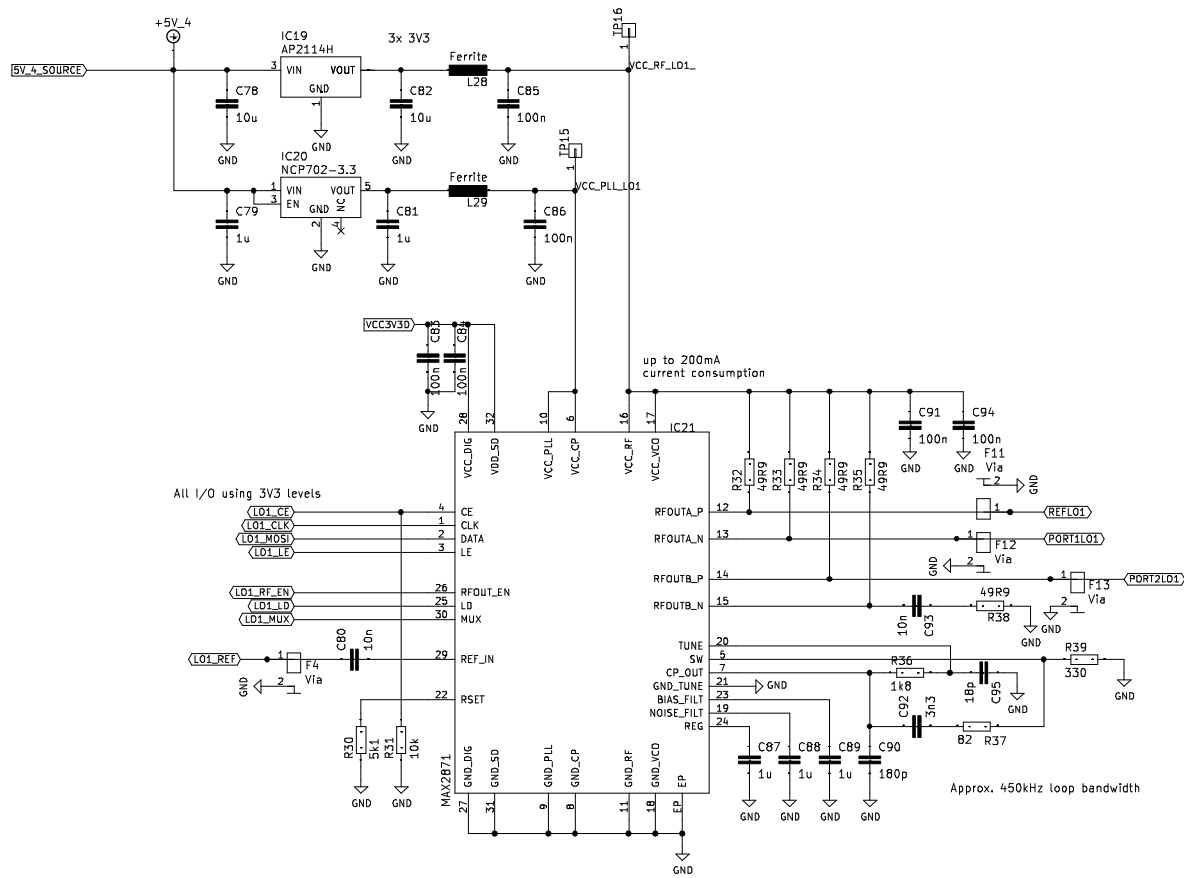
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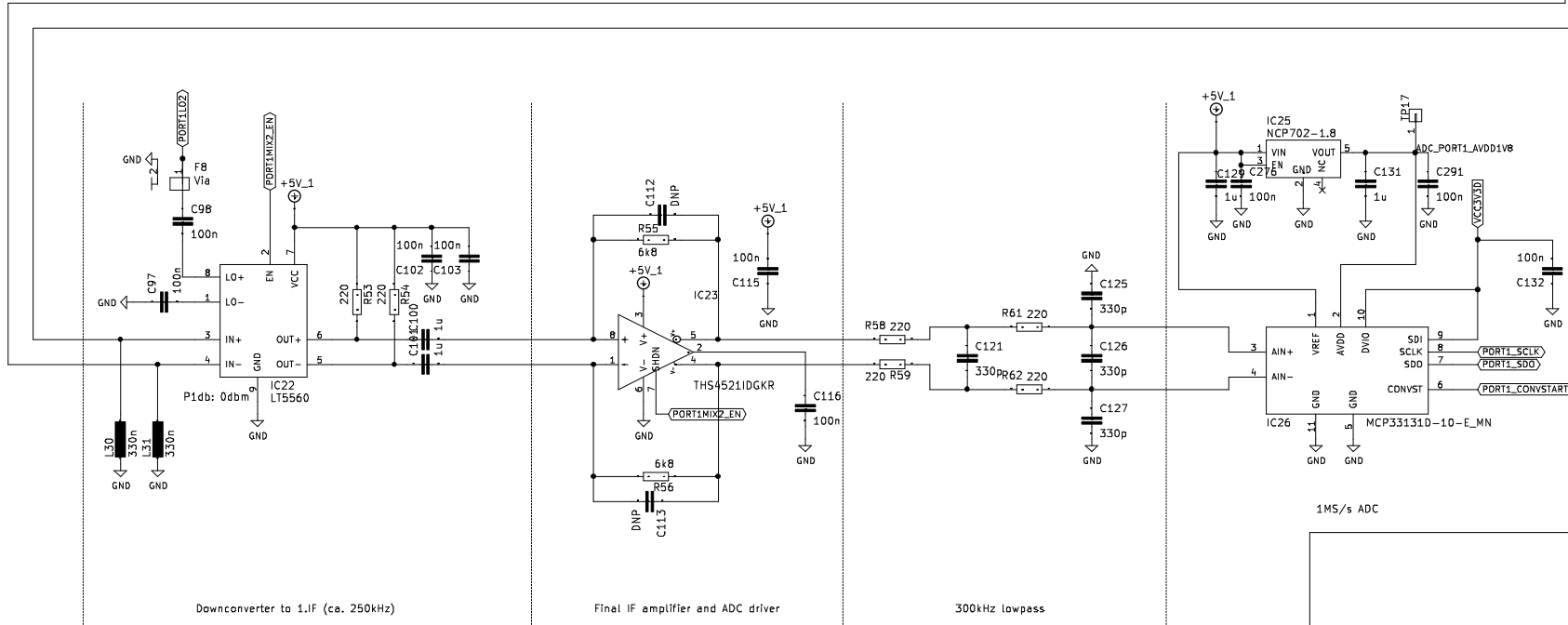
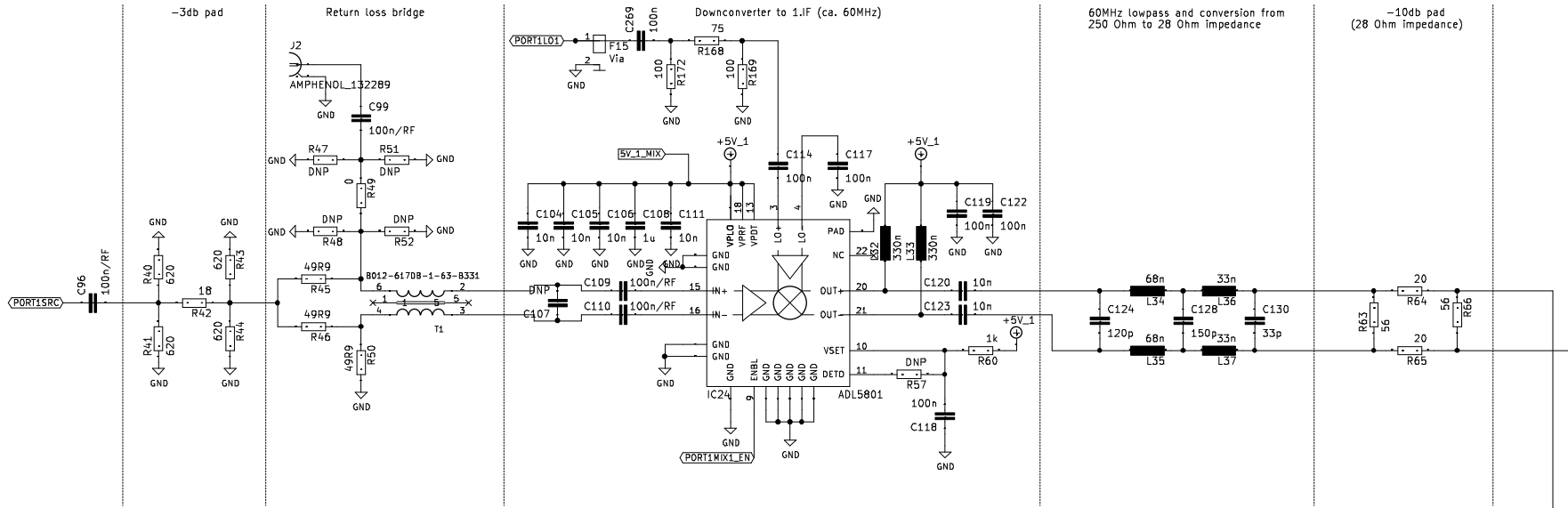
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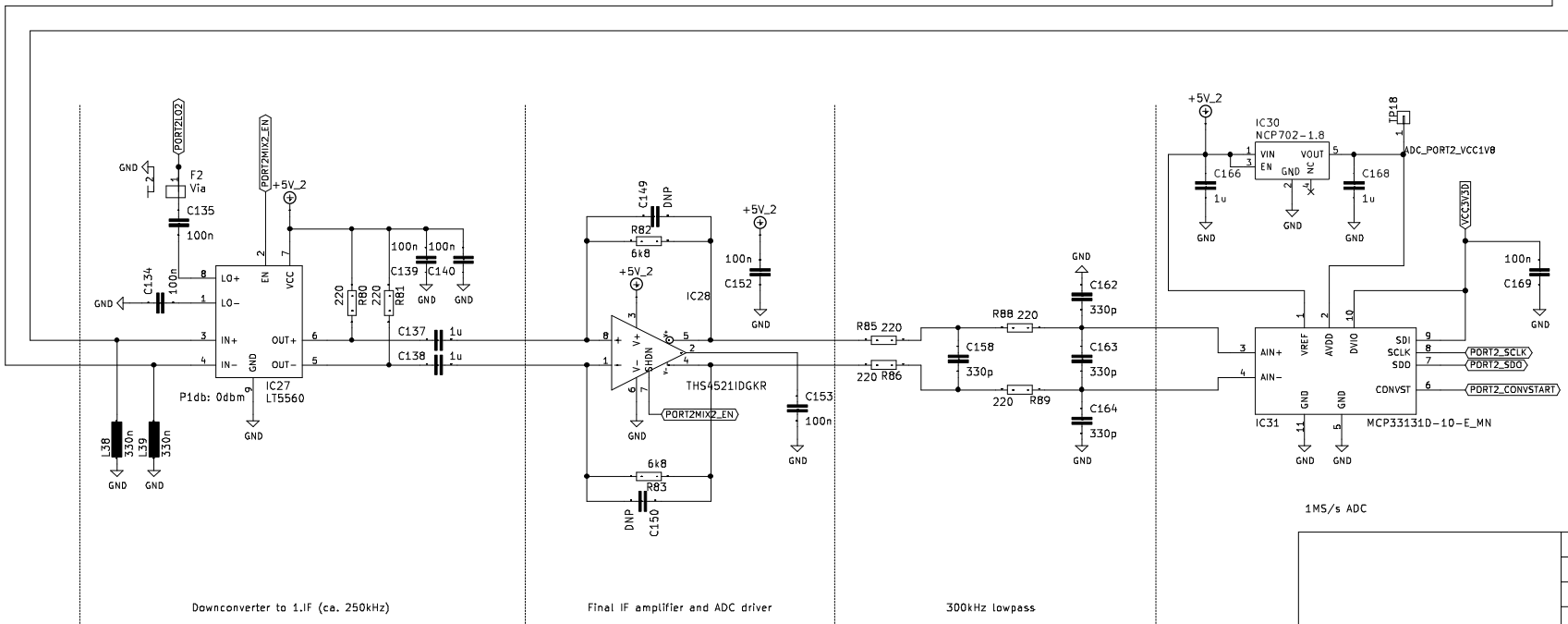
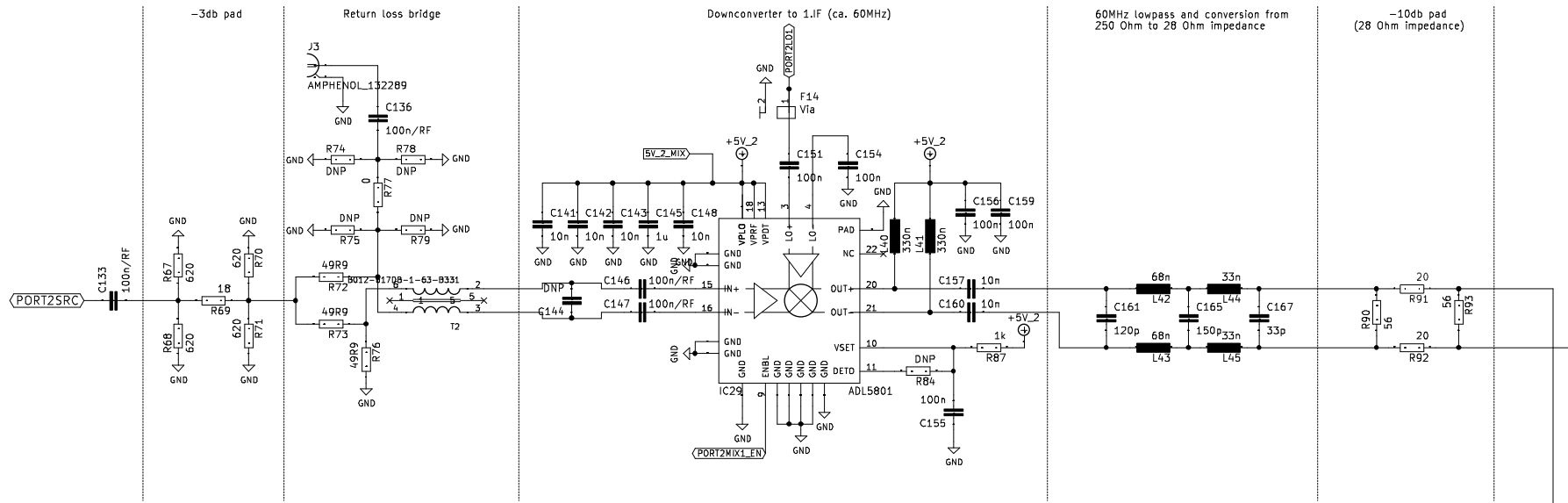
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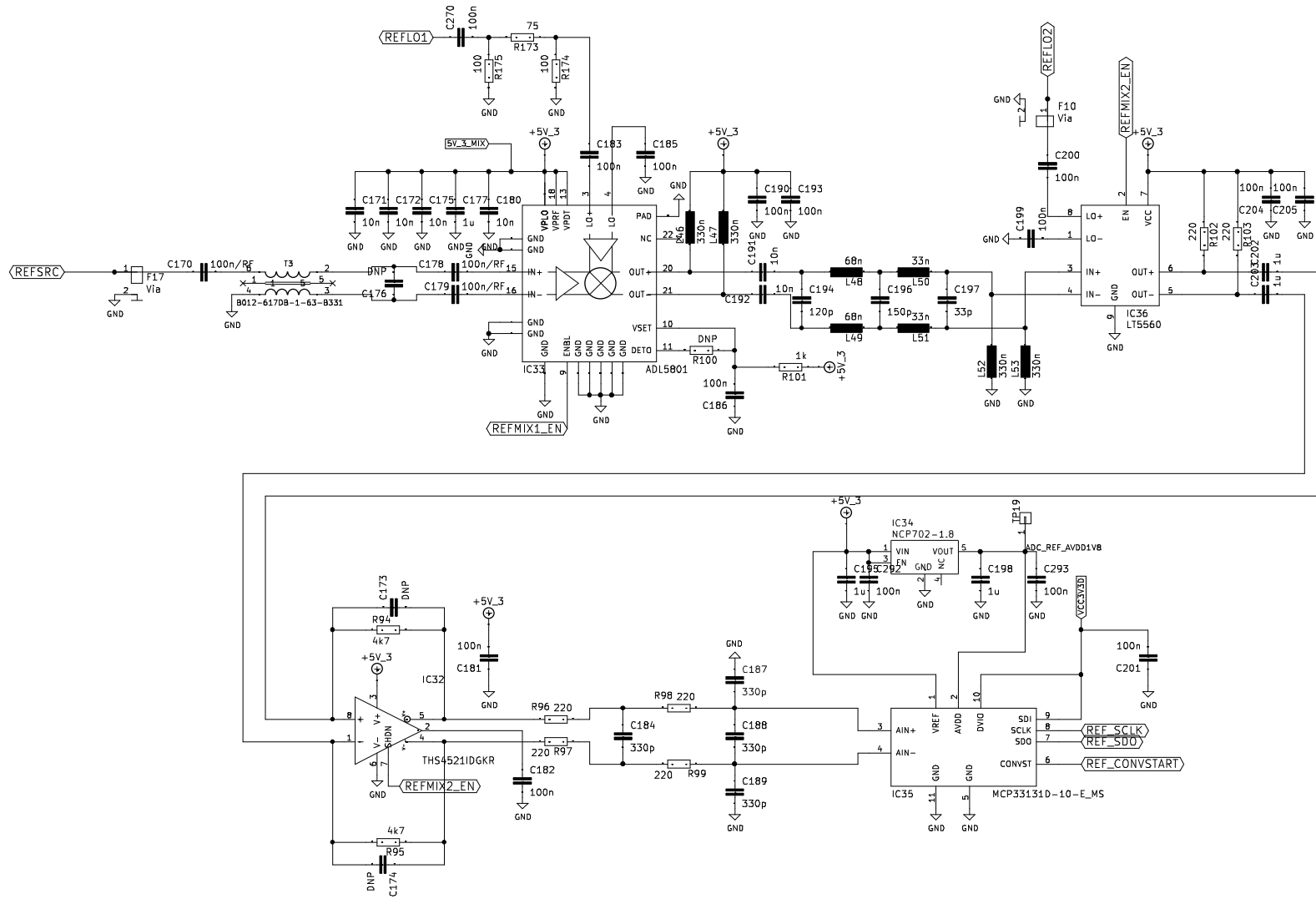


Port 1	>DRAWING_NAME
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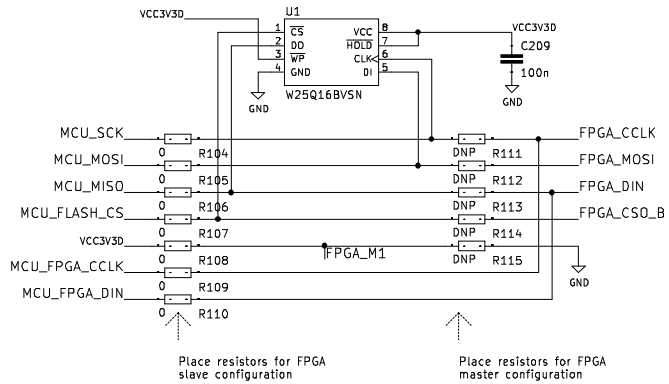


1MS/s ADC

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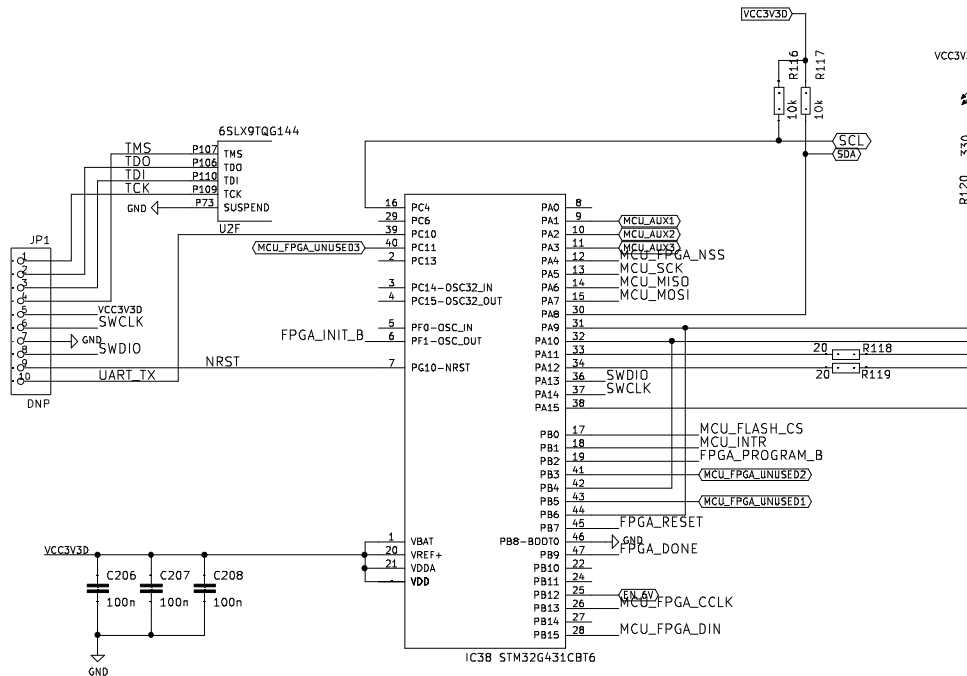
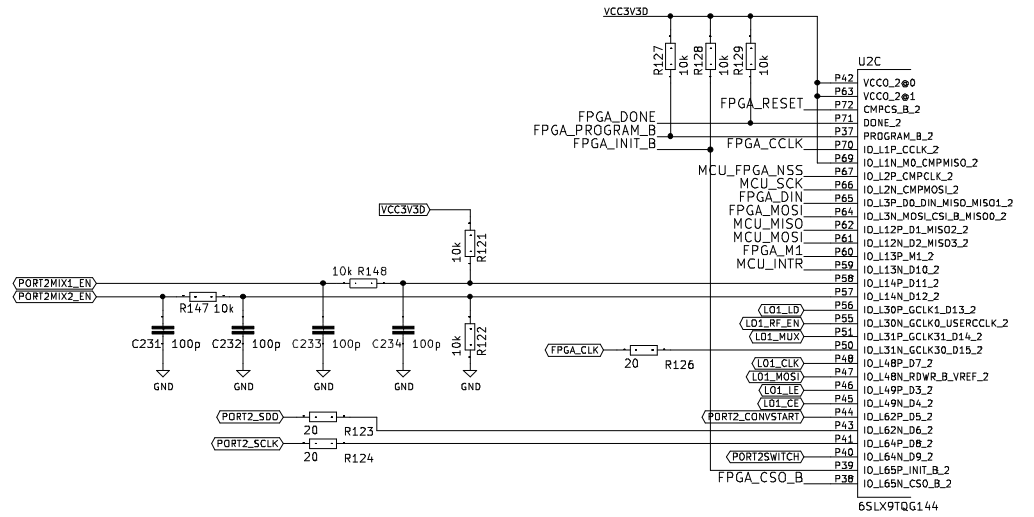


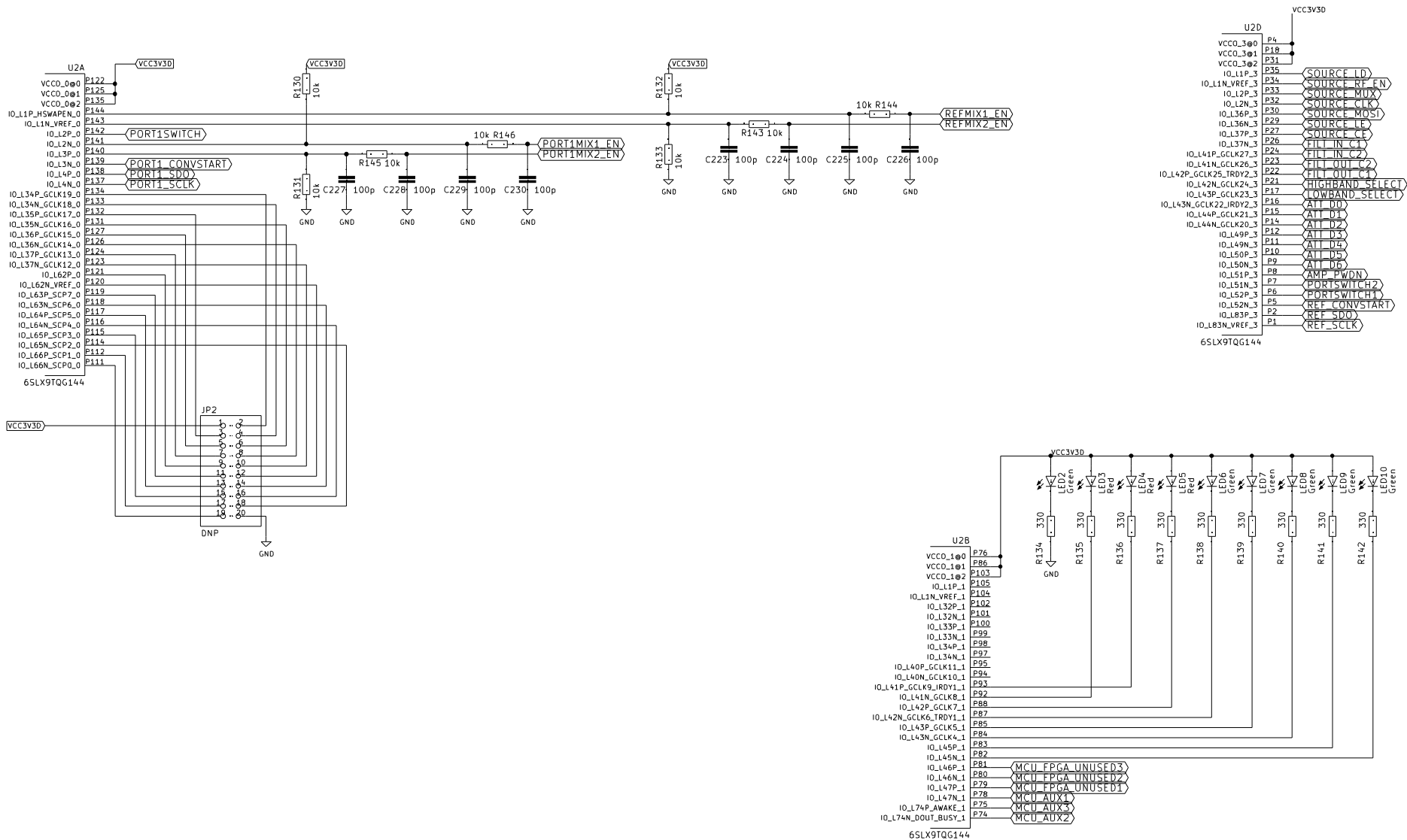
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Place resistors for FPGA slave configuration

Place resistors for FPGA master configuration





FPGA Connections	
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>LAST_DATE_TIME	
Sheet: >SHEET	