DATASHEET

Wi-Fi HaLow Sub-GHz Wireless Module

MM610X-001

Data Sheet

Rev. 2.0

Content

Revision Story

Version	Revision Date	Description	Initials	Approved
1.0	2022/10/5	Datasheet Release	Jeremy	Paul
2.0	2022/12/1	Information update	Jeremy	Paul

Description

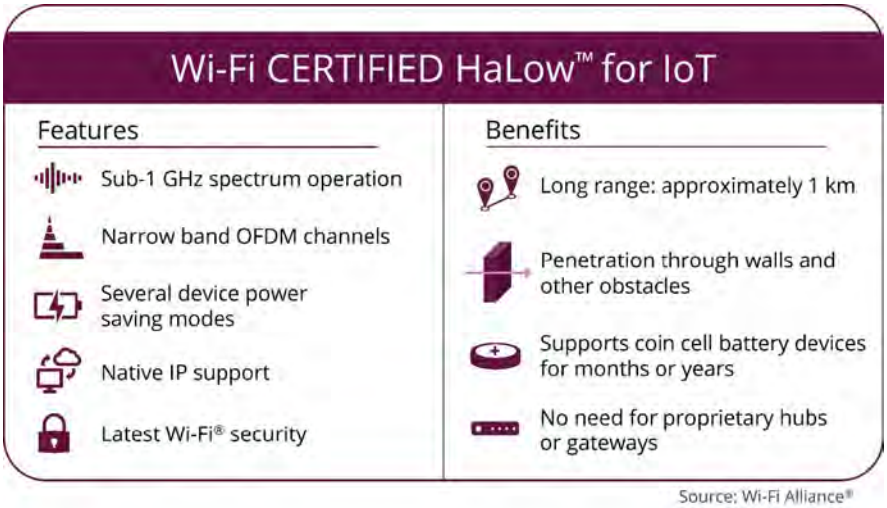
MM610X-001 is a Wi-Fi HaLow Sub-GHz wireless module based on the Morse Micro® MM6108 RF SOC. HaLow is a low-power, long-range version of the IEEE 802.11 Wi-Fi standard, designed for IoT applications.

The module operates below 1 gigahertz (GHz) and offers longer range and lower power connectivity. It complies with the Wi-Fi Alliance 802.11ah specification and is Wi-Fi CERTIFIED HaLow™. It provides excellent RF performance, with high sensitivity, selectivity, and blocking performance. The module also features a U.FL connector for an external Sub-GHz antenna.

It offers various IO interfaces including UART, SDIO, SPI, I2C, and GPIOs for PWM and switch functions. The module supports communication up to 2 kilometers Line of Sight (LOS), making it suitable for both indoor and outdoor IoT applications.

The MM610X-001 module delivers a UDP throughput of 20Mbps, offering superior capacity compared to other long-distance wireless IoT solutions. Its PHY data rate is 32.5Mbps. The module is certified with FCC, IC, CE, TELEC, NCC, and RCM.

In summary, the MM610X-001 module provides reliable and long-range connectivity for IoT applications, with excellent RF performance, versatile IO interfaces, and high throughput capabilities.



Features

Protocol

- 802.11ah OFDM PHY supporting future WFA HaLow certification
- BPSK & QPSK, 16-QAM & 64-QAM Modulation
- Automatic frequency & gain control
- Packet detect & channel equalization
- Forward Error Correction (FEC) coding & decoding
- Supports Modulation and Coding Scheme (MCS) levels MCS 0-7 and MCS 10
- Supports 1 MHz duplicate mode
- Supports optional Traveling Pilot
- 11ah MAC supporting future WFA HaLow certification
- Support for STA and AP roles
- Listen-Before-Talk (LBT) access with energy detect
- 11 power save
- 11 fragmentation and defragmentation
- Power-Saving Target Wake Time (TWT) support for long battery life
- Automatic and manual MCS rate selection

Radio Operation

- Single-stream max data rate of 32.5 Mbps (MCS=7, 64-QAM, 8MHz channel, 4 uSec GI)
- Radio supporting worldwide Sub-1 GHz frequency bands
- Frequency Range: 850-950 MHz
- Channel width options of 1/2/4/8 MHz

Transmitter Performance

- Tx output power (dBm): +21 dBm (Typical) MCS0

RF Interface

- External antenna connector

Power Consumption

- 37 mA RX current @ Listen
- 40 mA RX current @ Active Receive

Power Management Unit (PMU) for various modes of operation

- Power-down (interrupt driven wake)
- Hibernate mode (internal / external wake)
- Target Wake Time mode
- Active Receive / Transmit mode
- Integrated DC-DC converter supports a wide supply voltage, from 1.8V to 3.6V

Regulatory Certifications

- CE/FCC/IC/TELEC/RCM/NCC
- ESD: HBM 2KV / MM 200V, Latch-up: 150mA
- Halogen-free / RoHS 2.0 / Reach Annex 14 & 17

Certifications

- CE/FCC/IC/TELEC/RCM/NCC
- **FCC ID:** TKZMM610X-001
- **IC ID: 9968A-MM610X001;**

Operating Range

- 0-3.6V for VBATT and VDDFEM. 1.8-3.6V for VDDIO

  -40 to +85°C

Dimensions

- 22 mm x 17.0 mm x 2.0 mm (module)

Security

- AES encryption engine

- Hardware support for SHA1 and SHA2 hash functions (SHA-256, SHA-384, SHA-512)
- WPA3 including protected management frames (PMF)
- Opportunistic Wireless Encryption (OWE)

MCU Peripherals

- 12-bit 1 Msps SAR ADC
- 12 × GPIO
- 3 × UART, 1 x SPI, 1 x I2C
- 2 × 16-bit Timer/Counter
- 1 × 32-bit Timer/Counter
- 32-bit Real Time Counter
- 24-bit Low Energy Timer for waveform generation
- 2 × Watchdog Timer
- Power Management Unit for power state switching
- SDIO 2.0 compliant slave interface
- SDIO 2.0 Default Speed (DS) at 25MHz
- SDIO 2.0 High Speed (HS) at 50MHz
- Support for both 1-bit and 4-bit data mode
- Support for SPI mode operation

Applications

- Surveillance Cameras and Sensors
- Low-power Sensor Networks
- Asset Tracking and Management
- Building Access Control & Security
- Connected Toys and Games
- Agricultural and Farm Networks
- Proximity Sensors
- Smart Home Automation
- Appliances
- Smart Signs and Kiosks
- Vehicle-to-Vehicle Communications

- Biometric IDs and Keypads
- Intelligent Lighting Controls
- Wi-Fi to Wi-Fi HaLow Bridges
- Smart City Networks

Additional information

- Weight : 0.005 kg

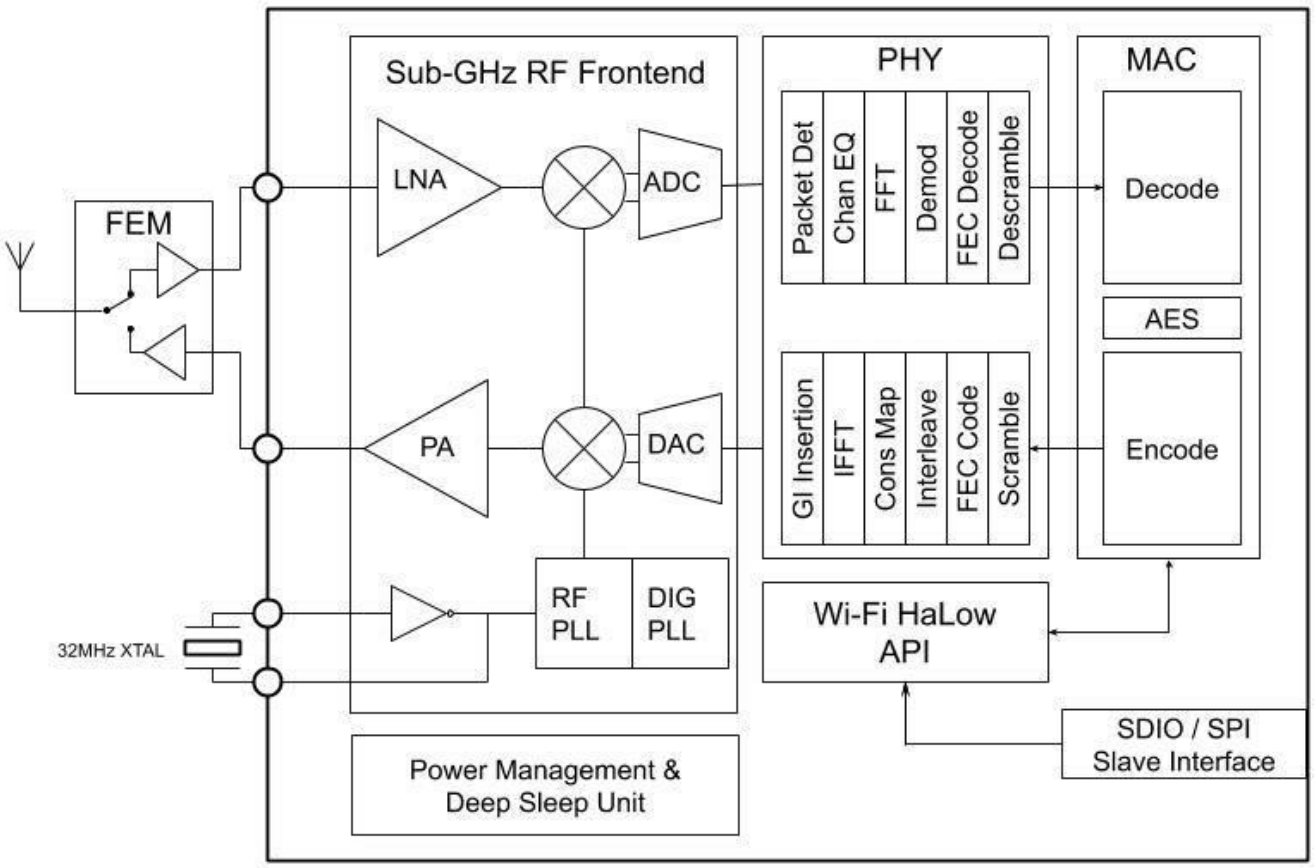
11ax related reading:

Introduction to 802.11ax High-Efficiency Wireless - NI

IEEE 802.11ax - Wikipedia

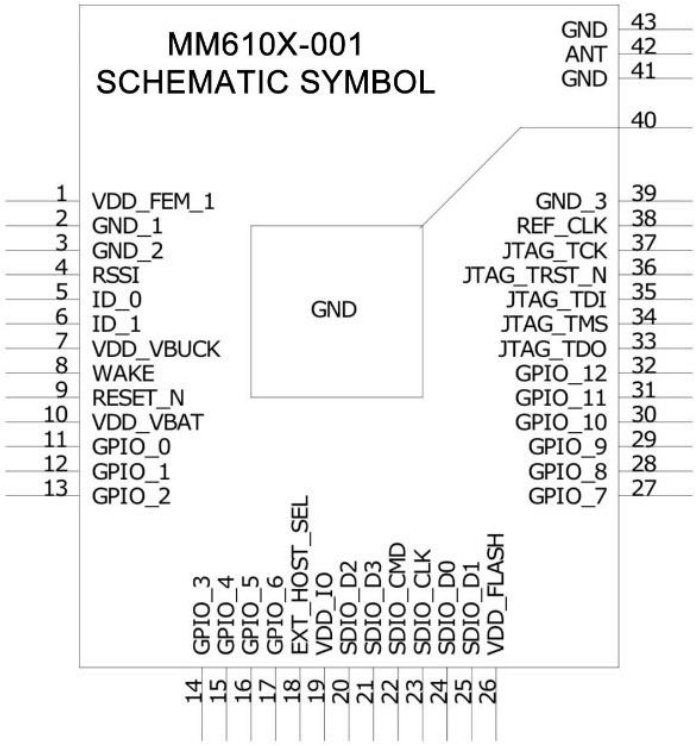
MM610X-001 Module Diagram

MM610x-001 SoC block diagram



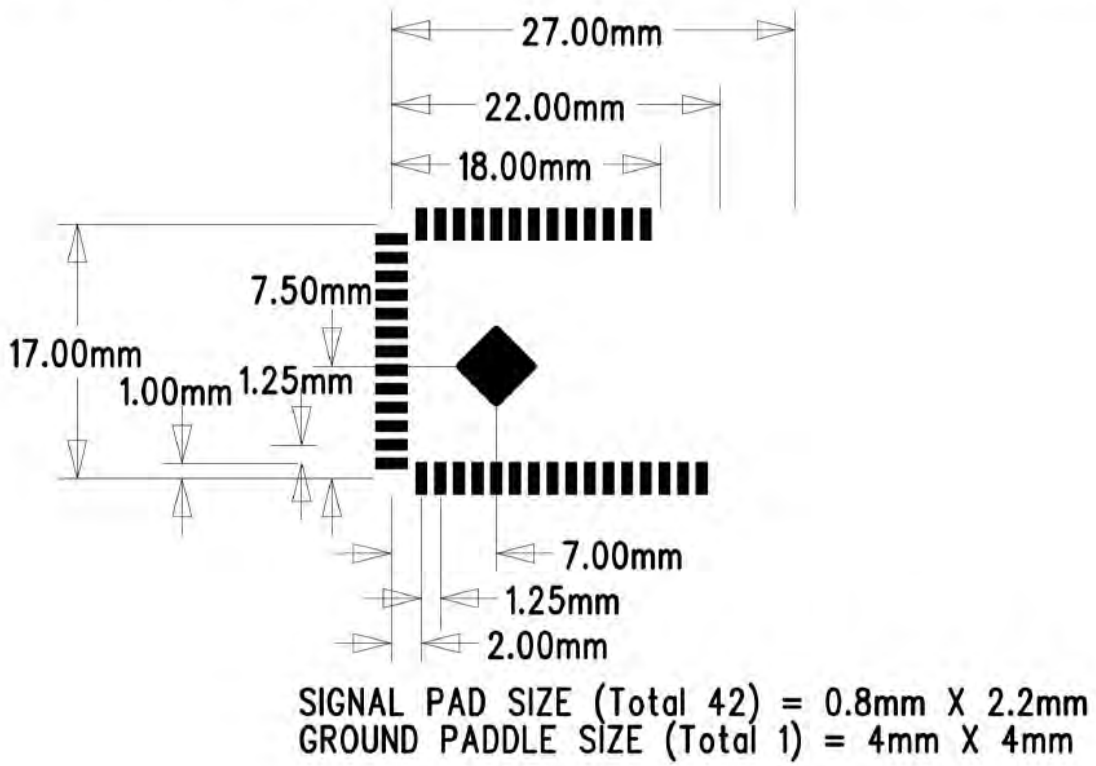
Module Pins Diagram

Remark: pin 42 could use to link antenna if ipex connector removed and add on 1 pcs 0Ω resister.

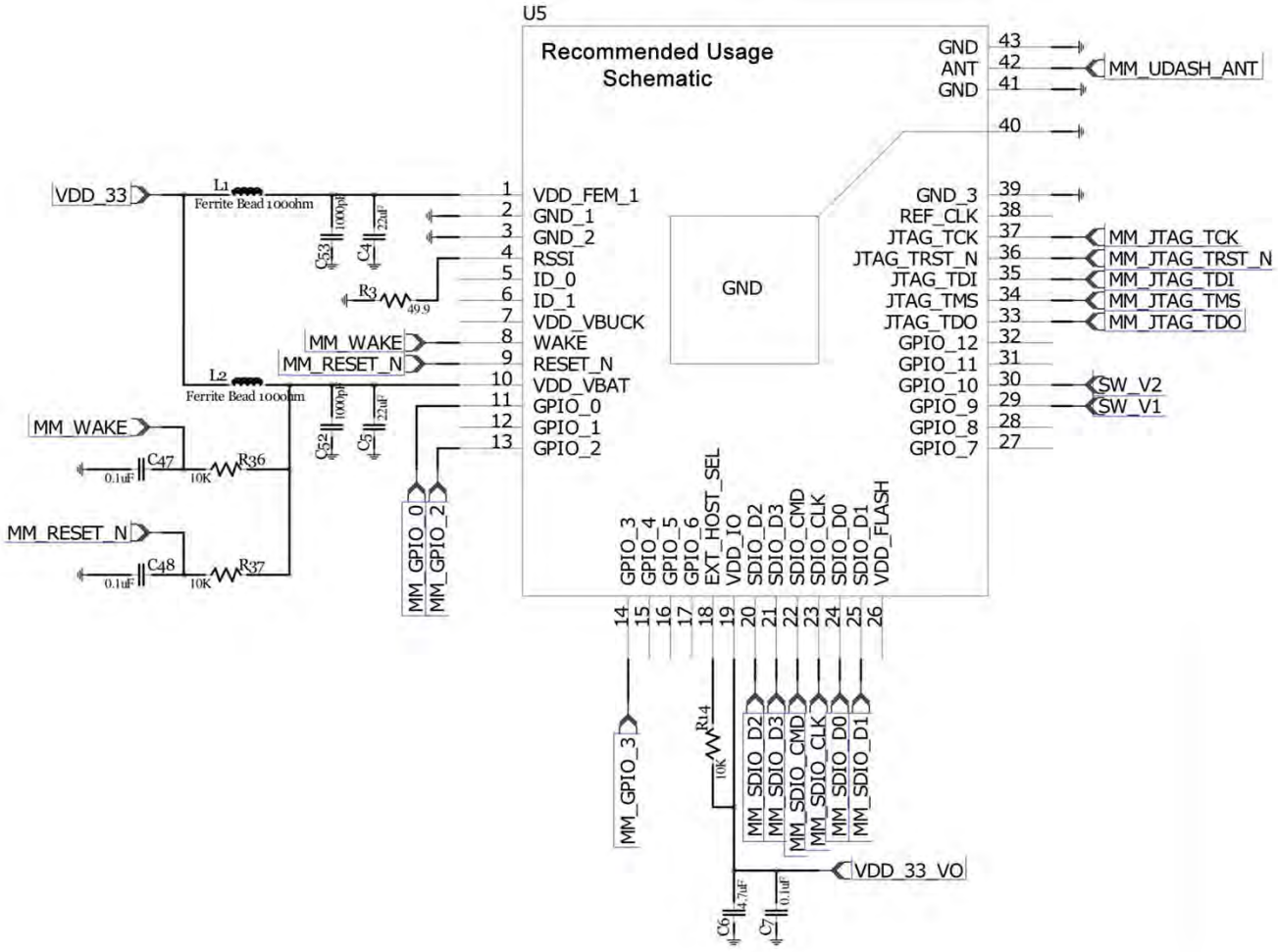


Module PCB PADs

PCB Footprint was updated to enlargen the pads from 0.8x1.1mm to 0.8x2.2mm



Recommended Usage Schematic



Pins Description

Pin	Name	Type	Primary Function	Alternate & Other Function(s)
1	VDD_FEM	Power	External PA/LNA power (3.3v)	
2	GND_1	Power	Ground	
3	GND_2	Power	Ground	
4	RSSI	O		
5	ID_0	O	Reserved	
6	ID_1	O	Reserved	
7	VDD_BUCK	Power	Reserved	
8	WAKE	I		
9	RESET_N	I		
10	VDD_VBAT	Power	Main module Power (3.3v)	
11	GPIO_0	I/O	General Purpose IO0	PWM1_0, SPI0_CS3
12	GPIO_1	I/O	General Purpose IO1	PWM1_1
13	GPIO_2	I/O	General Purpose IO2	UART0_RX, PWM1_2
14	GPIO_3	I/O	General Purpose IO3	UART0_TX, PWM1_3
15	GPIO_4	I/O	General Purpose IO4	I2C_SDA
16	GPIO_5	I/O	General Purpose IO5	I2C_SCL
17	GPIO_6	I/O	General Purpose IO6	UART1_RX
18	EXT_HOST_SEL	I	Mode selection	
19	VDD_IO	Power	3.3V VDD_IO Supply	
20	SDIO_D2	I/O	SDIO D2	
21	SDIO_D2	I/O	SDIO D3	
22	SDIO_CMD	I/O	SDIO CMD	
23	SDIO_CLK	I/O	SDIO CLK	
24	SDIO_D0	I/O	SDIO D0	
25	SDIO_D1	I/O	SDIO D1	
26	N.C.	Power	Reserved	
27	GPIO_7	I/O	General Purpose IO7	UART1_TX
28	GPIO_8	I/O	General Purpose IO8	SPI0_SCK
29	GPIO_9	I/O	General Purpose IO9	SPI0_CS0
30	GPIO_10	I/O	General Purpose IO10	SPI0_D0
31	GPIO_11	I/O	General Purpose IO11	
32	N.C.	I/O	Reserved	
33	JTAG_TDO	O	JTAG Data Out	
34	JTAG_TMS	I	JTAG Mode Select	
35	JTAG_TDI	I	JTAG Data In	
36	JTAG_TRST_N	I	JTAG Test Reset	
37	JTAG_TCK	I	JTAG Clock	
38	N.C.	I	Reserved	
39	GND_3	Power	Ground	
40	GND	Power	Ground	
41	GND	Power	RF Ground	
42	ANT	RF	RF signal launch pad	optional
43	GND	Power	RF Ground	

Electronic Specification

Item	Specification
RF Transmit Power	Tx output power (dBm): +21 dBm (Typical)
Power Consumption	37 mA RX current @ Listen 40 mA RX current @ Active Receive
Antenna	1 x UFL (IPEX) connector
PHY Rate	Upto 32.5Mbps
Physical Connectors	43 holes PCB board edge stamp holes
Operation Voltage	2.9V to 3.6V
Operation Temperature	-40 to 85 ℃
Security	WPA3
Interface	SDIO, SPI, GPIO

RF Receiver Sensitivity

MCS Index	Modulation Scheme	Coding Rate	Phy Rate (kbps) per BW				Spec Sensitivity (dBm) per BW			
			1MHz	2Mhz	4MHz	8MHz	1MHz	2Mhz	4MHz	8MHz
0	BPSK	1/2	333	722	1500	3250	-105	103	101	97
1	QPSK	1/2	667	1444	3000	6500	-102	100	97	93
2	QPSK	3/4	1000	2167	4500	9750	-99	97	95	92
3	16-QAM	1/2	1333	2889	6000	13000	-96	94	91	88
4	16-QAM	3/4	2000	4333	9000	19500	-93	90	88	85
5	64-QAM	2/3	2667	5778	12000	26000	89	87	84	81
6	64-QAM	3/4	3000	6500	13500	29250	88	85	83	80
7	64-QAM	5/6	3333	7222	15000	325500	87	84	81	78
10	BPSK	1/2 x 2	167	N/A			107	N/A		

Power Consumption

Transmit Power consumption

Mode	Condition T_A=25℃, V_{BAT}=V_{DDIO}=3.3V	VBAT Current (Typ)	V_{FEM} (Typ)	Unit
Transmit Current (MCS7, 16dBm, 100% D.C.)	1MHz channel	49	79	mA
	2MHz channel	54		mA
	4MHz channel	61		mA
	8MHz channel	74		mA
Transmit Current (MCS0, 21dBm, 100% D.C.)	1MHz channel	49	99	mA
	2MHz channel	54		mA
	4MHz channel	61		mA
	8MHz channel	74		mA

Receive Power Consumption

Mode	Condition TA=25℃, VBAT=VDDIO=3.3V	VBAT Current (Typ)	VFEM (Typ)	Unit
Listen	4MHz channel	26	4.5	mA
Active Receive	4MHz channel	32		mA

Sleep Power Consumption

Mode	Condition T_A=25℃, V_{BAT}=V_{DDIO}=3.3V	V_{BAT} Current (Typ)	Unit
Snooze	RTC On, Memory retained, configurable wake up timer	32.1	mA
Deep Sleep	RTC On, configurable wake up timer	1	mA
Hibernate	Power off, wait for external interrupt	1	1

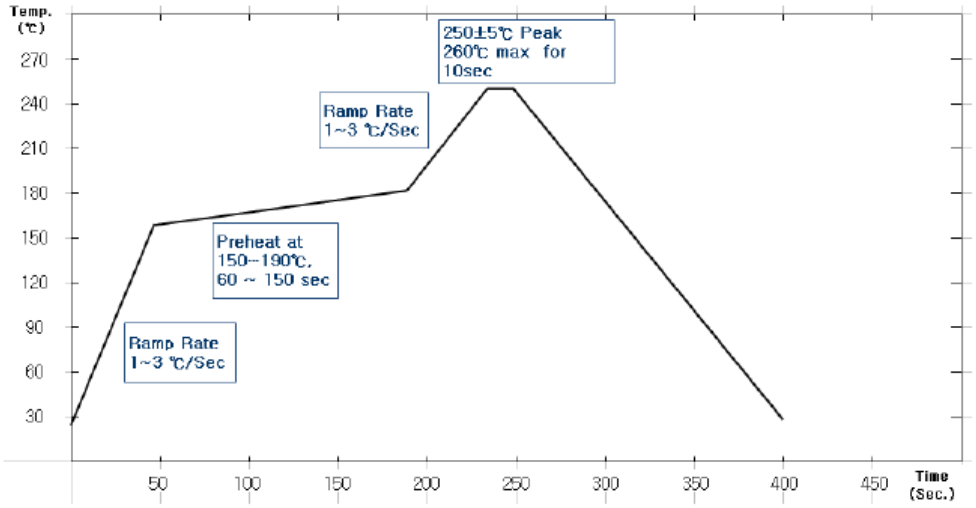
Ordering Information

Part Number	Description
MM610X-001	WiFi HaLow Module

Package

Tray plate: **To Be Discussed**

Reflow Profile



Electrical Characteristics

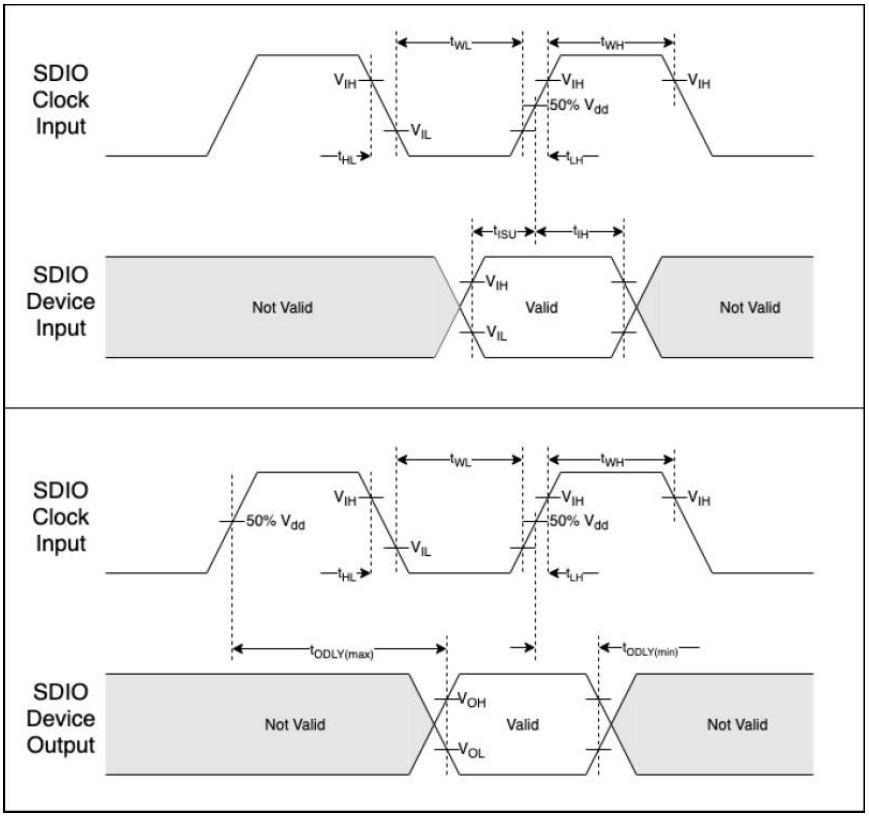
12.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD_FEM	Front End Module power input	-0.5	-	5.5	V
V_{BAT}	3.3V power supply	-0.5	-	4.3	V
V_{DDIO}	I/O supply Input	-0.5	-	4.3	V
Tstg	Storage temperature	-40	-	90	℃

12.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD_FEM	Front End Module power input	3.0	3.3	3.6	V
V_{BAT}	3.3V power supply	3.0	3.3	3.6	V
V_{DDIO}	3.3V I/O supply Input	1.8	3.3	V_{BAT}	V
TAMBIENT	Ambient temperature	TBD	TBD	TBD	℃

Timing Sequence



Parameter	Min	Max
Clock parameters		
Clock frequency	0MHz	50MHz
Clock low time (t_{WL})	7ns	
Clock high time(t_{WH})	7ns	
Clock rise time (t_{LH})		3ns
Clock fall time (t_{HL})		3ns
Inputs on CMD, DAT lines to device from host		
Input setup time (t_{ISU})	6ns	
Input hold time (t_{IH})	2ns	
Outputs on CMD, DAT lines from device to host		
Output delay ($t_{ODLY(max)}$)		14ns
Output hold time ($t_{ODLY(min)}$)	2.5ns	
Total system capacitance for each line		40pF

SDIO Bus Timing

The SDIO clock rate supports up to 50MHz. The device always operates in SD high speed mode.

SPI Bus

The SPI clock rate supports up to 50MHz. The SPI bus timing is identical to the SDIO bus timing, where MOSI and MISO are considered input and output timing, respectively, in the SDIO timing specification.

The SPI bus defaults to clock idling at logical 0 (CPOL=0), and data is launched and captured on the positive edges of the clock, as per SDIO high-speed mode. It may be configured to behave like CPHA=0 (drive output on negative edge, sample on positive edge) after being initialized.

UART Bus

Two universal asynchronous receiver/transmitter (UARTs) are available and provide a means for serial communication to off-chip devices. The UART cores are as-provided by the SiFive IP repository. The UART peripheral does not support hardware flow control or other modem control signals, or synchronous serial data transfers.

We will clock the UARTs with a maximum clock speed of 30MHz (TBD), meaning maximum baud of the UART will be around 30Mbaud or 30Mbits/s if a divisor of 0 is specified.

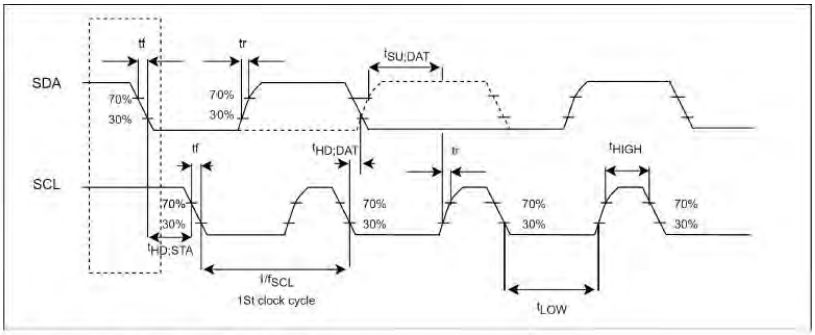
Pin	Name	Default Function	I/O Function
13	MM_GPIO2	GPIO	UART0 Tx
14	MM_GPIO3	GPIO	UART0 Rx
17	MM_GPIO6	GPIO	UART1 Tx
27	MM_GPIO7	GPIO	UART1 Rx

I2C Bus Timing

An I2C master interface is available. It consists of two lines, SDA and SCL, which are bidirectional, connected to a positive supply voltage via a current-source or pull-up resistor.

Pin	Name	Default Function	I/O Function
16	MM_GPIO5	GPIO	I2C SCL
15	MM_GPIO4	GPIO	I2C SDA

Definition of timing for F/S-mode devices on the I2C-bus. All value

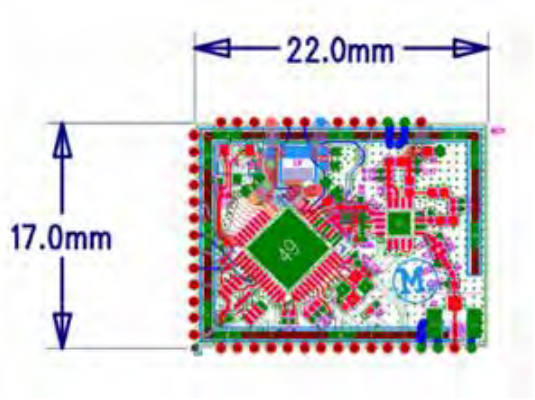


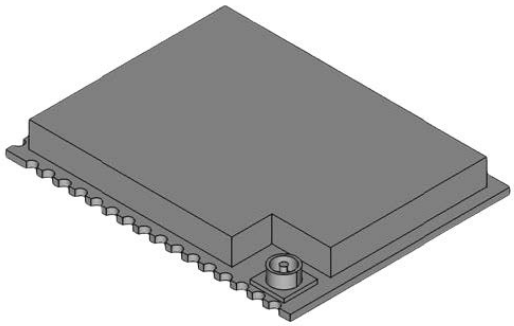
$V_{IH(min)}(0.3V_{DD})$ and $V_{IL(max)}(0.7V_{DD})$levels.

Parameter	Standard-mode		Fast-mode	
	Min	Max	Min	Max
Clock frequency(f_{SCL})	0	100kHz	0	400kHz
Fall time of both SDA and SCL (t_f)	-	300ns	20x (V_{DD}/5.5V)	300ns
Rise time of both SDA and SCL signals(t_r)	-	1000ns	20ns	300ns
Data hold time ($t_{HD;DAT}$)	5.0us	-	-	-
Data set-up time ($t_{SU;DAT}$)	250ns	-	100ns	-
LOW period of the SCL clock	4.7us	-	1.3us	-
HIGH period of the SCL clock	4.0us	-	0.6us	-
Hold time- START,first clock is generated after this($t_{HD;STA}$)	4us	-	0.6us	-

Mechanical Information

Mechanical Drawing





Application Design Note

To Be Discussed