# FM6363C（文件编号：S&CIC1989） 16 路 EPWM 恒流输出 LED 驱动 IC

## 简介

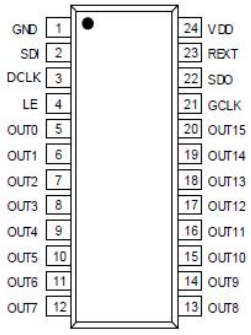
FM6363C 是专为 LED 全彩显示屏应用设计的驱动芯片。FM6363C 内建 16 位位移缓存器可以将串行的输入资料转换成每个输出通道的灰阶像素。FM6363C 的 16 个恒流输出通道所输出的电流值不受输出端负载电压影响，提供一致并且恒定的输出电流，不受 PCB 板的影响，具有极佳的抗干扰性。FM6363C 不仅可以由不同阻值的外接电阻来调整各输出级的电流大小，而且还可以由软件来调整的 FM6363C 通道电流增益从而控制 LED 显示屏亮度。FM6363C 采用富满 EPWM 专利显示技术，采用智能脉冲宽度调变功能，增强了低灰视觉效果。

FM6363C 可支持 33-64 扫 LED 扫描屏；通过技术创新可以有效解决低灰色块、偏色、麻点、第一行偏暗、高对比耦合、跨版色差等问题；透过实时错误侦测功能，FM6363C 不需增加额外的外部原件即可独立侦测每个 LED 是否为开路状态；FM6363C 新颖的消除十字架现象功能，解决了因 LED 坏点造成的周遭灯点错误显示问题。此外，FM6363C 内建的消隐/钳位电路配合不同的配置位，可以大幅度增强消隐/钳位的能力，有效解决了上下鬼影和文字鬼影现象；具有耦合优化增强功能，能极大改善跨版耦合、高对比、中对比耦合等各种显示瑕疵；更有黑屏节能功能，降低黑屏时的功耗。

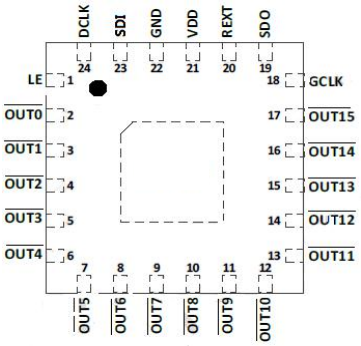
## 特性

- 工作电压：VDD=3.3V~5.5V
- 恒流输出范围值：
  - 在 5 伏特操作电压：0.5~25mA
  - 在 4.2 伏特操作电压：0.5～18mA
  - 在 3.3 伏特操作电压：0.5~10mA
- 极为精确的电流输出值：
  - 通道间最大差异值：<±2%
  - 芯片间最大差异值：<±2%
- 内建 12 位 SRAM 内存支持 33~64 扫分时多任务扫描
- EPWM 灰阶控制技术提升低灰视觉效果（富满专利）
- 8 位电流增益调整，12.5%~200%
- 有效改善跨版耦合、高对比耦合问题
- 恒流拐点 8 档可调
- LED 故障排除：
  - 消除 LED 坏点造成的十字架现象
  - LED 开路侦测
- 内建消隐，消隐增强
- 快速输出电流响应时间（OE）最小值：20ns@VDD=5V
- GCLK 倍频技术
- 黑屏节能，降低黑屏功耗
- 工作温度范围：Topr=-40～85℃
- 高达 30MHz 时钟频率
- 封装形式：SSOP-24(e=0.635mm)
  - AN：QFN-24-4×4-0.5mm
  - BN：QFN-24-4×4-0.5mm

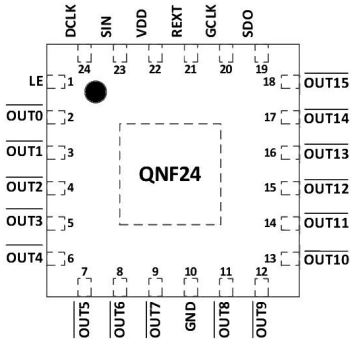
## 管脚图




SSOP-24




AN：QFN-24




BN： QFN-24

**PAGE 1 Paragraph 1**

FM6363C is a driver chip specially designed for LED full-color display applications. FM6363C built-in 16-bit shift register can convert serial input data into each output.

The grayscale pixels of the channel. The current value output by the 16 constant current output channels of FM6363C is not affected by the load voltage at the output end, providing a consistent and constant output current that is not affected by the PCB.

It has excellent anti-interference performance. FM6363C can not only adjust the current of each output stage through external resistors with different resistance values, but also adjust it by software.

FM6363C channel current gain to control LED display brightness. FM6363C adopts Fuman EPWM patented display technology and adopts intelligent pulse width modulation function to enhance the Low gray visual effect.

**Paragraph 2**

FM6363C can support 33-64 LED scanning screens; through technological innovation, it can effectively solve low gray blocks, color casts, pitting, dark first lines, high contrast coupling, and cross-page colors.

differential problem; through the real-time error detection function, FM6363C can independently detect whether each LED is open circuit without adding additional external components; FM6363C novel

The function of eliminating the cross phenomenon solves the problem of incorrect display of surrounding light points caused by dead LED pixels. In addition, FM6363C's built-in blanking/clamping circuit cooperates with different configuration bits.

It can greatly enhance the blanking/clamping capabilities, effectively solving the phenomenon of upper and lower ghosting and text ghosting; it has coupling optimization and enhancement functions, which can greatly improve cross-version coupling, high contrast, medium

Contrast coupling and other display defects; it also has a black screen energy-saving function to reduce power consumption when the screen is black.

**PAGE 1 BULLET LEFT LIST**

Working voltage: VDD=3.3V~5.5V

Constant current output range value:

Operating voltage at 5 volts: 0.5~25mA

Operating voltage at 4.2 volts: 0.5~18mA

Operating voltage at 3.3 volts: 0.5~10mA

Extremely accurate current output value:

Maximum difference between channels: <±2%

Maximum difference between chips: <±2%

Built-in 12-bit SRAM memory supports 33~64 scan time-sharing multi-task scanning

 EPWM gray scale control technology improves low gray visual effects (Fuman patent)

 8-bit current gain adjustment, 12.5%~200%

Effectively improve cross-version coupling and high-contrast coupling issues

 Constant current inflection point adjustable in 8 levels

**PAGE 1 BULLET RIGHT LIST**

LED troubleshooting:

Eliminate the cross phenomenon caused by LED dead pixels

LED open circuit detection

 Built-in blanking, blanking enhancement

 Fast output current response time (OE) minimum: 20ns@VDD=5V

 GCLK frequency multiplication technology

 Black screen energy saving, reduce black screen power consumption

 Working temperature range: Topr=-40～85℃

 Up to 30MHz clock frequency

Package form: SSOP-24(e=0.635mm)

AN: QFN-24-4×4-0.5mm

BN: QFN-24-4×4-0.5mm

## 管脚功能描述

| 管脚名称 | 功能说明 |
|---|---|
| GND | 接地端。 GROUND TERMINAL |
| SDI | 串行数据输入端。 SERIAL DATA INPUT |
| DCLK | 数据时钟讯号之输入端。 DATA CLOCK SIGNAL INPUT TERMINAL |
| LE | 数据闪控(data strobe)输入端。 DATASTROBE INPUT TERMINAL |
| $-\overline{OUT0}\sim\overline{OUT15}$ | 恒流输出端。 CONSTANT CURRENT OUTPUT TERMINAL |
| GCLK | 灰阶时钟讯号输入端。GRAY SCALE CLOCK SIGNAL INPUT TERMINAL |
| SDO | 串行数据输出端。 SERIAL DATA OUTPUT |
| R-EXT | 连接外接电阻之输入端；此外接电阻可设定所有输出通道之输出电流。 |
| VDD | 电源端。 POWER TERMINAL |

CONNECTTHE INPUT TERMINAL OF AN EXTERNAL RESISTOR. THIS EXTERNAL RESISTOR CAN SET THE OUTPUT CURRENT ALL ALL OUTPUT TERMINALS

## 功能框图
FUNCTIONAL BLOCK DIAGRAM

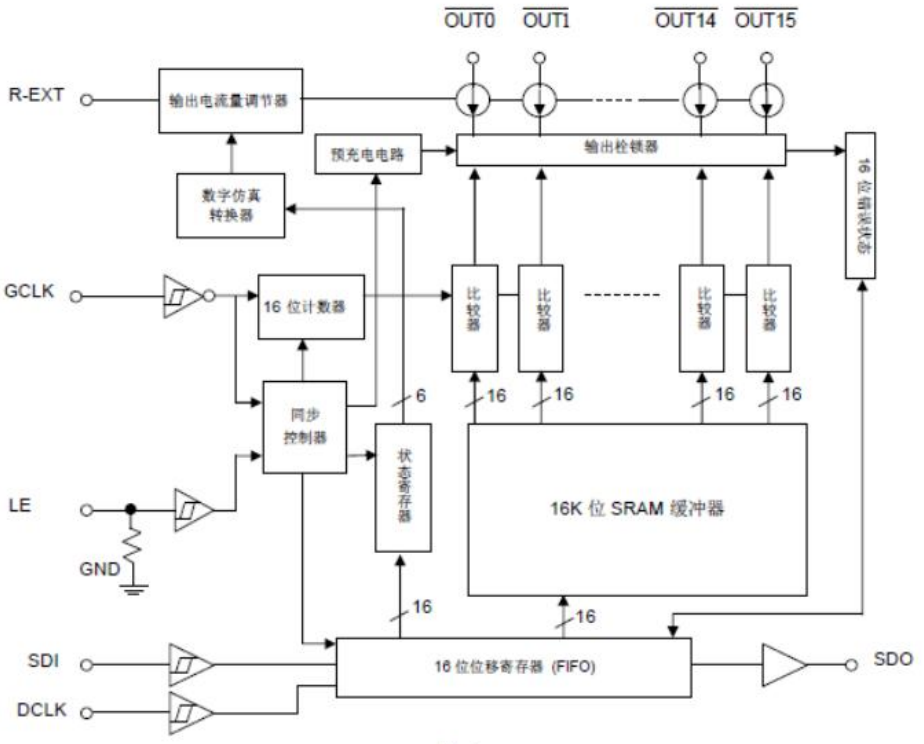
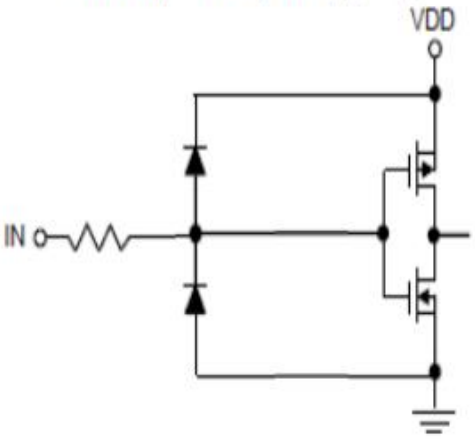


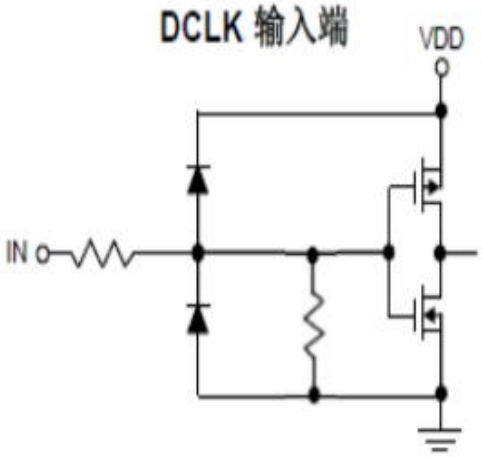

图 1

## 输出输入等效电路
**OUTPUT INPUT EQUIVALENT CIRCUIT**

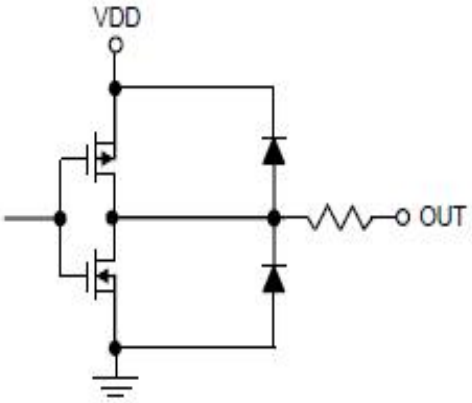
GCLK, LE , SDI 输入端




DCLK 输入端




SDO 输出端



## 最大限定范围 MAXIMUM RANGE

| 特性 | | 符号 | 范围 | 单位 |
|---|---|---|---|---|
| 电源电压 VOLTAGE | | $V_{CC}$ | 0~6 | V |
| 输入端电压(SDI, CLK, LE, GCLK) INPUT TERMINAL VOLTAGE | | $V_{LED}$ | -0.4~$V_{DD}$ +0.4 | V |
| 输出端耐受电压 OUTPUT TERMINAL WITHSTAND VOLTAGE | | $V_{DS}$ | -0.5~11 | V |
| 输出端电流 OUTPUT CURRENT | | $I_{OMAX}$ | +25 | mA |
| 接地端电流 GROUND TERMINAL CURRENT | | $D_{IO}$ | 500 | mA |
| 消耗功率 (在四层印刷电路板上，25°C 时)* | GP 包装 | $P_D$ | 3.12 | W |
| | GFN 包装 | | 1.79 | |
| 热阻值 (在四层印刷电路板上，25°C 时)* | GP 包装 | $R_{th(j-a)}$ | 40.01 | °C/W |
| | GFN 包装 | | 69.5 | |
| 接合点温度 | | $T_{j,max}$ | 150** | °C |
| 芯片工作时的环境温度 | | $T_{opr}$ | -40~+85 | °C |
| 芯片储存时的环境温度 | | $T_{stg}$ | -55~+150 | °C |

*模拟时，PCB 尺寸为 76.2mm*114.3mm。请参考 JEDEC JESD51 规范。

**越接近此最大范围值操作，芯片的寿命越短、可靠度越低；超过此最大限定范围工作时，将会影响芯片运作并造成毁损，因此建议的芯片工作时的接合点温度在 125° C 以内。

注: 散热表现与散热片尺寸、PCB 厚度与层数息息相关。实测的热阻值会与模拟值不相同，使用者可选择适当的封装与 PCB 布局，以达到理想的散热表现。

**When simulated, PCB size is 76.2mm*114.3mm. Please refer to the JEDEC JESD51 specification.**
****The closer the operation is to this maximum range value, the shorter the life of the chip and the lower the reliability; when operating beyond this maximum limit range, it will affect the operation of the chip and cause damage, so the recommended junction temperature for chip operation is within 125°C.**

**Note: Thermal performance is closely related to the heat sink size, PCB thickness and number of layers. The measured thermal resistance value will be different from the simulated value. The user can select the appropriate package and PCB layout to achieve ideal thermal performance.**

## 直流特性（$V_{DD}$=5.0V，Ta=25℃）

所有测试条件皆为电流增益调整设置为默认值

When each channel is turned on, all test conditions are current gain adjustment and set to default values.

*一个通道开启时所有测试条件皆为电流增益调整设置为默认值

| 特性 | | 符号 | 量测条件 | 最小值 | 一般值 | 最大值 | 单位 |
|---|---|---|---|---|---|---|---|
| 输出端耐受电压 | | $V_{DS}$ | $\overline{OUT0}$ ~ $\overline{OUT15}$ | - | - | 11.0 | V |
| 输入端电压 | 高电位位准 | $V_{IH}$ | Ta=-40~85° C | 0.7×$V_{DD}$ | - | $V_{DD}$ | V |
| | 底电位位准 | $V_{IL}$ | Ta=-40~85° C | GNG | - | 0.3×$V_{DD}$ | V |
| 输出端漏电流 | | $I_{OH}$ | $V_{DS}$ =11.0V | - | - | 0.5 | μA |
| 输出端电压 | SDO | $V_{OH}$ | $I_{OH}$=-1.0mA | $V_{DD}$-0.4 | - | - | V |
| | | $V_{OL}$ | $I_{OL}$=+1.0mA | - | - | 0.4 | V |
| 电流偏移量（通道间） | | $dI_{OUT1}$ | | - | ±1.5 | ±2.0 | % |
| 电流偏移量（芯片间） | | $dI_{OUT2}$ | | - | ±1.5 | ±2.0 | % |
| 电流偏移量 VS.输出电压* | | %/$dV_{DS}$ | $V_{DS}$ 介于 1.0V 与 3.0V 之间, $R_{ext}$ =1.3KΩ@7mA | - | ±0.1 | - | %/V |
| 电流偏移量 VS.电源电压* | | %/$dV_{DD}$ | $V_{DD}$ 介于 4.5V 与 5.5V 之间, $R_{ext}$ =1.3KΩ@7mA | - | ±0.1 | - | %/V |
| 下拉电阻 | | $R_{IN}$ (down) | DCLK | | 240 | | KΩ |
| 电压源输出电流 | “关” (SDI=DCLK=GCLK =0Hz) | $I_{DD}$(off) 1 | $R_{ext}$ =Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ =Off | - | 4 | – | mA |

*一个通道开启时

## 动态特性（T = 25℃，$V_{DD}$ = 5.0V）

| 特性 | | 符号 | 量测条件 | 最小值 | 一般值 | 最大值 | 单位 |
|---|---|---|---|---|---|---|---|
| 设定时间 **set time** | SDI-DCLK ↑ | $t_{SU0}$ | $V_{DD}$=5.0V<br>$V_{IH}$=VDD<br>$V_{IL}$=GND<br>$R_{ext}$=1.3KΩ<br>$V_{DS}$=1V<br>$R_L$=300Ω<br>$C_L$=10pF<br>$C_1$=100nF<br>$C_2$=10μF<br>$C_{SDO}$=10pF<br>$V_{LED}$=4.0V | 3 | - | - | ns |
| | LE ↑ – DCLK ↑ | $t_{SU1}$ | | 7 | - | - | ns |
| 保持时间 **hold time** | DCLK ↑ - SDI ↓ | $t_{H0}$ | | 3 | - | - | ns |
| | DCLK ↑ - LE ↓ | $t_{H1}$ | | 7 | - | - | ns |
| **delay** 延迟时间 | DCLK – SDO | $t_{PD0}$ | | - | 25 | - | ns |
| **pulse width** 脉波宽度 | LE | $t_{w(LE)}$ | | 15 | - | - | ns |
| **Potential rise time of current output port** 电流输出埠的电位爬升时间 | | $t_{OR}$ | | - | 25 | 35 | ns |
| **Potential fall time of current output port** 电流输出埠的电位下降时间 | | $t_{OF}$ | | - | 25 | 35 | ns |

## 直流特性的测试电路

**Test circuit for DC characteristics**

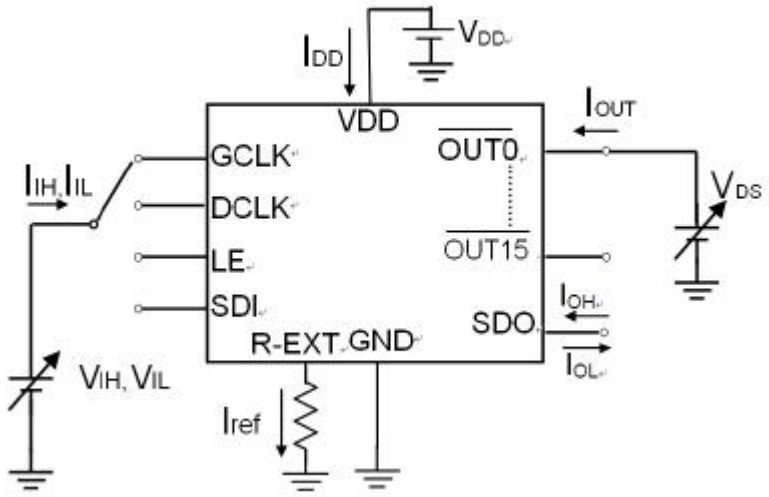



图 2

## 动态特性的测试电路
**Dynamic Characteristics Test Circuit**

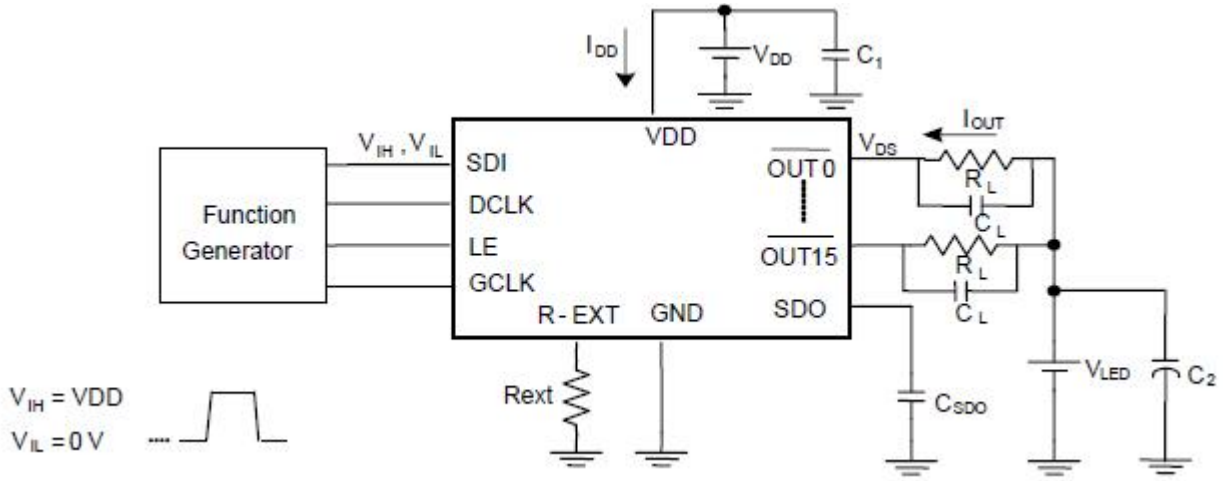
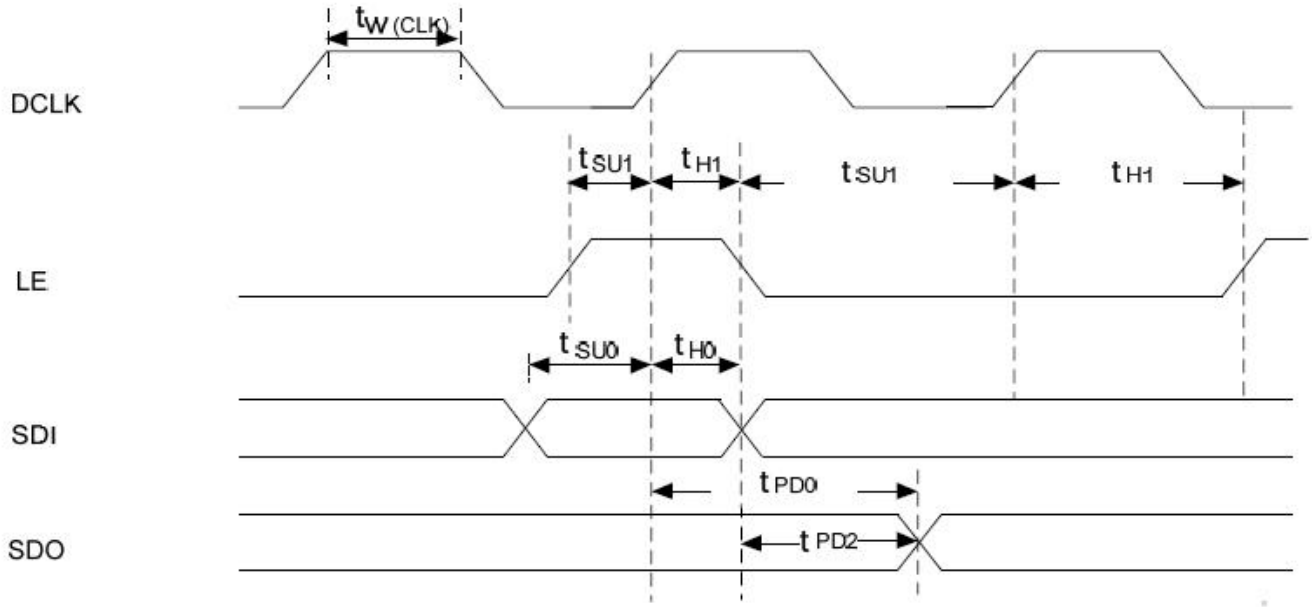
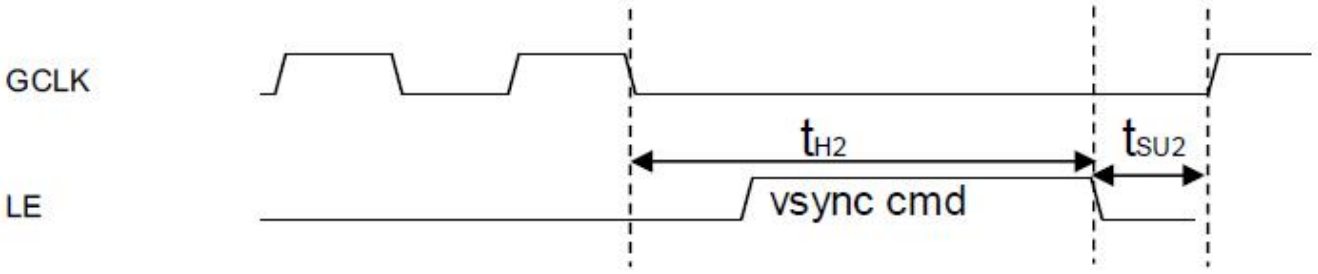



图 3

## 时序的波形图
**Timing waveform diagram**




（1）

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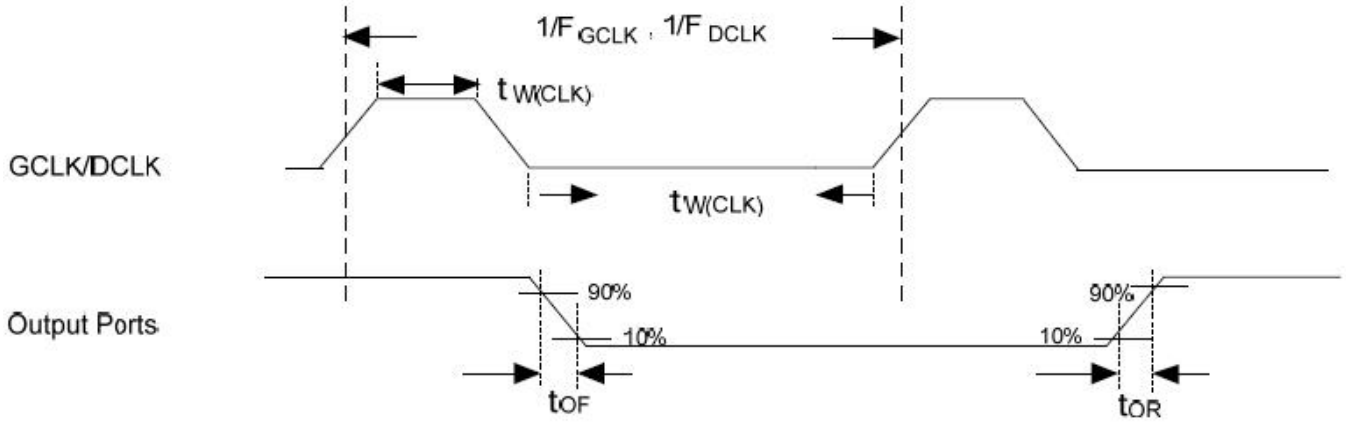



（3）

## 操作原理 Operating principle

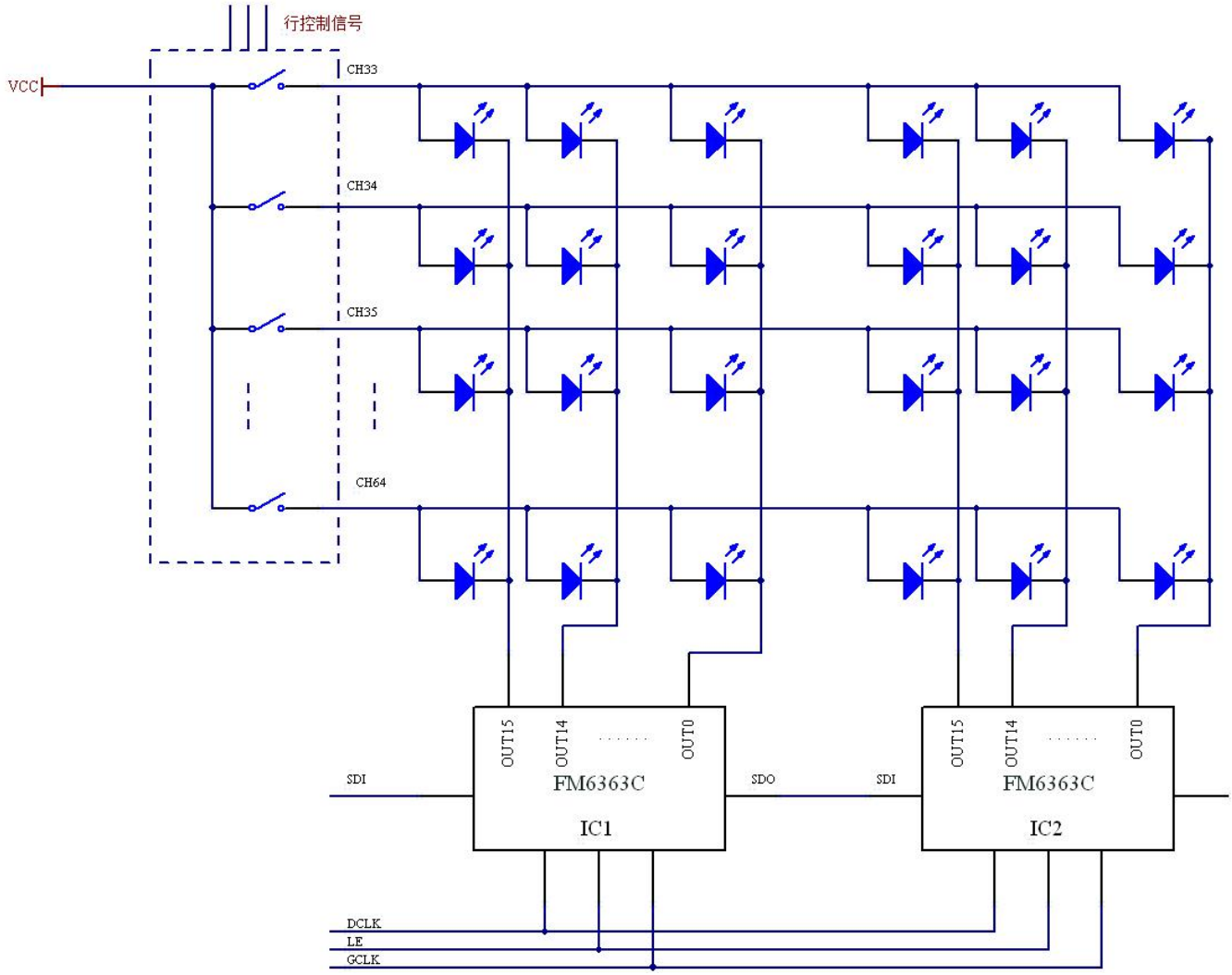
下图显示扫描行数为 64 行扫描屏所建议的应用架构图。由 LE 与 DCLK 组成的指令，可透过 SDI 与 SDO 脚位来传送灰阶数据。16 个输出通道( OUT0~ OUT15)会在不同时间点传递 PWM 数据给每个扫描行数，因此必须具备时间多任务操作的开关给每行之扫描。

**The figure below shows the recommended application architecture diagram for a 64-line scanning screen. Instructions composed of LE and DCLK can be sent through SDI and SDO pins**

**Grayscale data. The 16 output channels (OUT0~ OUT15) will transmit PWM data to each scanning line at different time points, so they must have time multi-tasking capabilities.**

**Switch to scan each line.**

扫描屏应用架构 **Scan screen application architecture**




**FM6363C adopts precise current control technology, which can achieve minimal difference in current between channels and even between chips.**

**1. The maximum current difference between channels is less than ±2.0%, and the maximum current difference between chips is less than ±2.0%.**

## 应用信息

**2. It has current output characteristics that are not affected by the load terminal voltage. It is recommended that the minimum channel voltage (Vout_min) reference value for the chip to maintain a constant output current is as follows, Vout_min=VDS+Iout*10, where VDS is an internal parameter of the chip and can be configured through registers. The typical value is 0.29V, so the constant current inflection point of the chip is 0.30V@Iout=10mA.**

FM6363C 采用精确的电流控制技术，可以做到通道与通道间，甚至芯片与芯片间的电流，差异极小。

1、 通道间的最大电流差异小于±2.0%，而芯片间的最大电流差异小于±2.0%。

2、 具有不受负载端电压影响的电流输出特性，建议芯片维持恒定输出电流的最低通道电压（Vout_min）参考值如下，Vout_min= VDS+Iout*10, 其中，VDS 为芯片内部参数，可通过寄存器配置，典型值为 0.29V，故芯片的恒流拐点为 0.30V@Iout=10mA。

输出电流 IOUT，藉由外接一个电阻 Rext ，配合寄存器调节 VREXT 电压来设定输出电流。

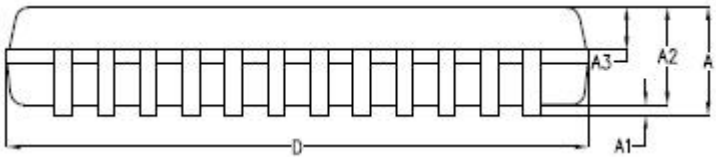
Iout= （Vrext/Rext）*9.9 其中，Vrext 表示 Rext 端口的电压值，可由芯片内部的寄存器配置电压值（建议配置的 VREXT 电压不低于 0.3V）Rext 是指外接至 R-EXT 端的电阻值，9.9 代表电流的放大系数。

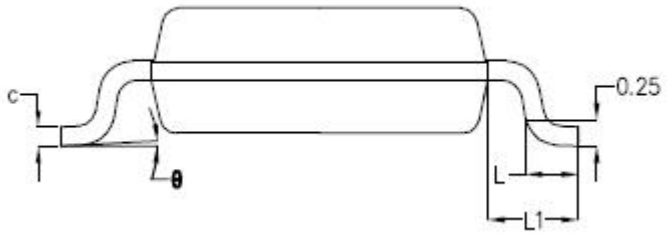


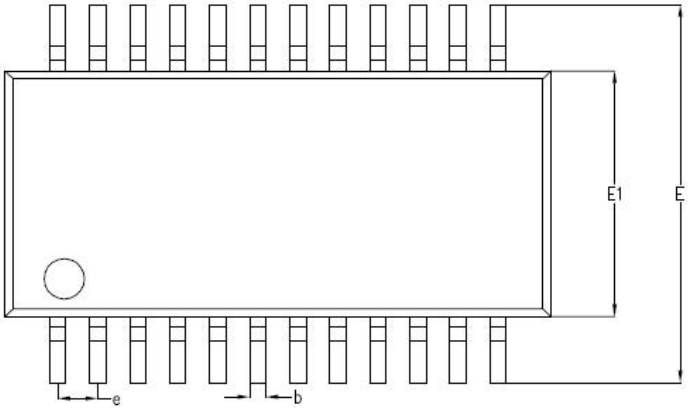
**Iout= (Vrext/Rext)*9.9 Among them, Vrext represents the voltage value of the Rext port. The voltage value can be configured by the register inside the chip (it is recommended to configure the VREXT voltage Not less than 0.3V) Rext refers to the resistance value externally connected to the R-EXT terminal, and 9.9 represents the current amplification factor.**

## 封装信息

SSOP24（0.635）

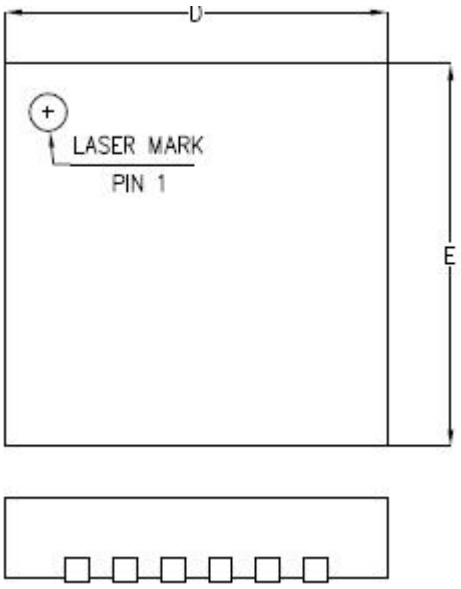


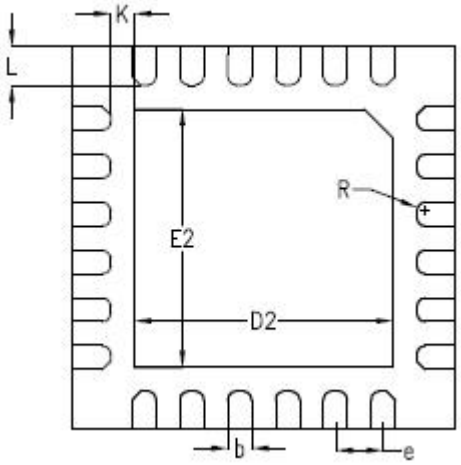



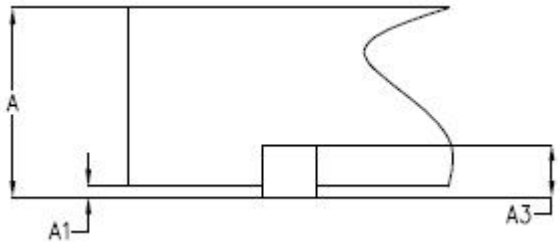




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | 1.60 | 1.65 |
| A1 | - | 0.15 | 0.20 |
| A2 | 1.40 | 1.45 | 1.50 |
| A3 | 0.60 | 0.65 | 0.70 |
| b | 0.22 | 0.25 | 0.30 |
| c | 0.17 | 0.22 | 0.25 |
| D | 8.55 | 8.65 | 8.75 |
| E | 5.90 | 6.00 | 6.10 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | 0.635BSC | | |
| L | 0.57 | 0.60 | 0.65 |
| L1 | 1.05BSC | | |
| θ | 0° | 3° | 6° |

QFN-24-4×4（0.5mm）




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.83 | 0.85 | 0.87 |
| A1 | 0 | 0.02 | 0.05 |
| A2 | – | | |
| A3 | 0.20REF | | |
| b | 0.18 | 0.25 | 0.30 |
| D | 3.90 | 4.00 | 4.10 |
| D2 | 2.65 | 2.70 | 2.75 |
| E | 3.90 | 4.00 | 4.10 |
| E2 | 2.65 | 2.70 | 2.75 |
| e | 0.40 | 0.50 | 0.60 |
| K | 0.25REF | | |
| L | 0.35 | 0.40 | 0.45 |
| L1 | – | – | – |
| **R** | 0.09 | – | – |