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Characterization of deep traps in the near-interface oxide of widegap metal–oxide–semiconductor interfaces revealed by light irradiation and temperature change

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To evaluate oxide trap state density in the near-interface region of silicon carbide metal–oxide-semiconductor (SiC MOS) stacks, photo-assisted capacitance–voltage measurements at various temperatures were performed. The difference between the deep trap profiles at SiC MOS interfaces treated with two kinds of post-oxidation-annealing was revealed, which cannot be detected by conventional evaluation methods of interface state density. With this method, the differences in the energy profile of trap levels together with their spatial distribution in the near interface region of oxide were investigated. © 2022 The Japan Society of Applied Physics

1. Introduction

The wide-bandgap semiconductors such as silicon carbide (SiC) are expected as the next-generation materials for high-voltage power devices and other applications such as high-temperature operatable complementary metal–oxide–semiconductor devices. However, the performance of those devices expected from their physical properties of them has not been achieved mainly due to the lack of optimized fabrication processes. For example, the characteristics of SiC metal–oxide–semiconductor field-effect-transistors (MOSFETs) are seriously degraded by the effects of the high density of defects at the MOS interfaces.[1] These defects cause problems such as low channel mobility and low reliability of the device operation. Therefore, suppressing the density of the traps near the MOS interface and improving its electrical properties is crucially important to improve the SiC MOSFET performance.

A serious concern is that in such widegap materials many of those interface defect states near the MOS interface may not be detected and quantified by conventional methods, such as interface state density (D_{it}) evaluation.[2] In general, the shallow traps, which locate in the energetically and spatially shallow region can be detected and quantified by the D_{it} evaluation method, while the fixed charge density can be quantified from the flat band voltage (V_{fb}) shift observed in the capacitance–voltage (C–V) characteristics. As shown in Fig. 1, since fixed charges and shallow traps are dominant in the Si MOS interface, conventional methods are enough to evaluate the interface quality. However, for wide gap materials, there are some kinds of traps that are often overlooked in those conventional methods, such as deep interface traps and near interface traps located in the oxide layer. The latter ones are called near-interface traps (NITs),[3,4] which often appear in various non-Si MOS interfaces.

Among various common polymorphs of SiC, 4H-SiC has a larger bandgap of 3.26 eV and higher bulk electron mobility which does not depend on its crystal orientation significantly.[5,6] So, it has attracted much attention for power device applications even though the performance expected from its physical properties of it has not been achieved. A part of such performance limitation can be attributed to the high density of NITs. Especially the NIT with deep levels are

often overlooked. For example, in SiC MOSFETs the low reliability is a problem, such as a threshold voltage instability when a voltage is continuously applied. It is believed that this is mainly due to the effect of the trapped electrons or holes located away from the interface in the oxide film.[7] Actually, a bias temperature instability measurement study[8] indicates the existence of a large amount of NITs, which results in the observation of recovery of V_{th} after the release of bias stress.[9] Therefore, a characterization method of NITs with deep levels is needed.

To characterize the profile of NITs, it is crucial to evaluate both energy distribution and spatial distribution of them in the oxide. Even though the hysteresis width of C–V characteristics is often regarded as one of the indicators of the quantity of slow time-constant traps, it has not been easy to analyze the energy distribution and spatial distribution separately. Therefore, in this study, we propose and demonstrate a method that can evaluate oxide trap density located in the near-interface region, which can distinguish the energy profile and the spatial depth profile of them in the oxide. The energy profile of the oxide traps is quantified from the photo-assisted C–V measurement where the wavelength of the light is continuously changed. On the other hand, the spatial depth profile of them is evaluated by conducting the photo-assisted C–V measurements at various temperatures. A part of this study has been already reported in the extended abstract of the 2021 International Workshop on Dielectric Thin Films for Future Electron Devices 2021[10] using only the samples fabricated on p-type 4H-SiC substrates. On the other hand, by using the samples fabricated on both p- and n-type 4H-SiC substrates, this paper discusses totally the difference of the profiles of the traps in the near interface region among different annealing processes.

2. Experimental methods

Both 8°-off axis 4H-SiC (0001) substrates covered with Al-doped p-type epitaxial layer (doping density $\sim 1.3 \times 10^{16}$ cm^{-3}) and 4°-off axis 4H-SiC (0001) substrates with n-type epitaxial layer (doping density $\sim 1.1 \times 10^{16}$ cm^{-3}) were employed in this study. After HF cleaning, the wafers were oxidized in dry-O$_2$ ambient at 1300 °C to grow SiO$_2$ films (~ 25 nm) thermally, followed by either of two kinds of post-oxidation annealing processes: (i) re-oxidized in H$_2$O + O$_2$ ambient (pH$_2$O:pO$_2$ = 9:1) at 800 °C for 8 h (wet-POA), or
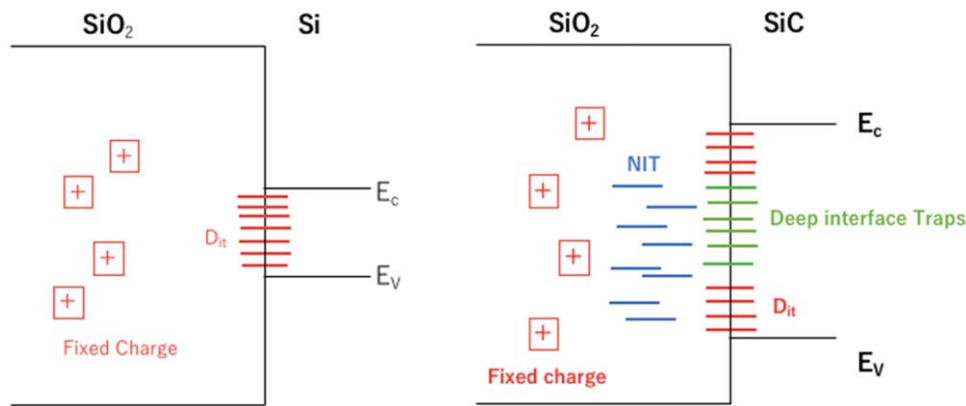
Fig. 1. (Color online) Schematic of differences of both energetic and spatial distributions of the trap states exiting near the MOS interfaces, between Si MOS and widegap semiconductors MOS stacks.

(ii) $N_2 + NO$ ambient (N_2:NO = 2:1) at 1150 °C for 8 h (NO-POA). We compared the effects of those two kinds of annealing processes conducted after conventional thermal oxidation of SiC to examine the validity of our evaluation methods. Various approaches to improving the MOS interface characteristics of 4H-SiC MOSFETs have been studied so far, for example, high-temperature thermal oxidation,[11] NO or N_2O annealing after dry oxidation,[12,13] and so on. Among those methods, the introduction of nitrogen by a NO annealing process after oxidation (NO-POA) is the most common SiC surface passivation technique.[14] On the other hand, the H_2O-oxidation processes on 4H-SiC have been also reported to result in better interface characteristics[15–17], especially for PMOSFETs.[18] Our group has also demonstrated that post-oxidation annealing in H_2O-including ambient environment (wet-POA) at a temperature as low as 800 °C works quite efficiently for both n-type and p-type.[18–20] Therefore, those two kinds of POA processes, NO-POA and wet-POA were chosen to demonstrate the effectiveness of the evaluation methods proposed in this study.

After two kinds of POA processes, Au was vacuum evaporated as a gate electrode to fabricate MOS capacitors. The gate area was $\sim 5 \times 10^{-5}$ cm^2. The photo-assisted C–V measurements were performed at room temperature (300 K) and low temperature (223 K, and 173 K) with 1 MHz, while changing the photon energy of light through a monochromator, from 1.6 to 3 eV with an energy step of 0.2 eV (at 300 K) and from 1.6 to 2.8 eV with energy step of 0.4 eV

(at 223 K and 173 K), respectively, using Xe lamp as the light source. The significant difference in energy steps is due to the limitation of experimental facilities. The gate voltage-sweeping rate in the C–V measurements was ~ 100 mV s^{-1}. The light with around ~ 0.8 Wcm^{-2} was irradiated on the sample for 180 s, while a depletion bias was applied. Immediately after stopping the irradiation, the gate voltage sweep started from the depletion state toward the accumulation state, then from accumulation to the depletion state. The hysteresis width of the C–V curve of this voltage cycle was evaluated.

3. Photo-assisted C–V with various wavelengths of light

3.1. Principle of photo-assisted C–V with various wavelengths of light

In photo-assisted C–V measurements, the occupancy ratio of the deep levels is forcibly changed by the light irradiation under a depletion bias. After stopping the irradiation, C–V measurement is conducted where the density of deep level traps can be quantified from the hysteresis width of the C–V curve because the trapped charges are once excited by the light irradiation in the depletion state, but re-captured when the accumulation bias is applied.[21–23] In this study, we continuously change the wavelength of light to estimate the energy distribution of deep levels. The trap energy level that should be forced to become vacant by light can be tuned by changing the wavelength as schematically shown in Fig. 2 for
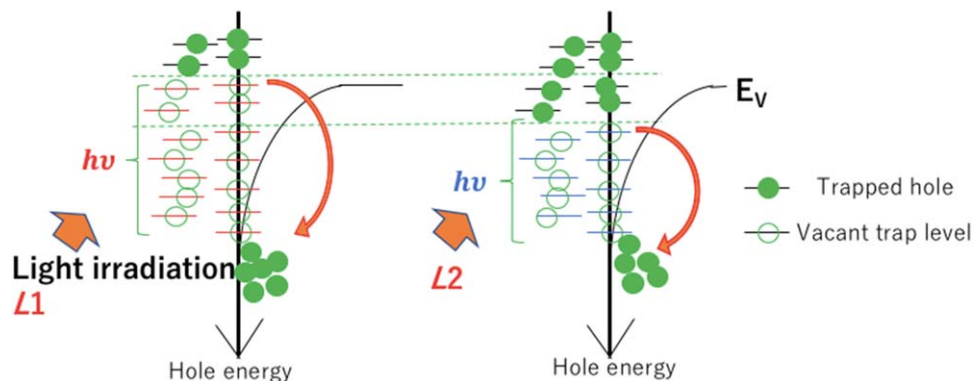

Fig. 2. (Color online) Schematic diagram to indicate the energy levels of traps whose charges are excited by light irradiation, drawn for the cases of irradiating different light wavelengths, $L1$ and $L2$, respectively, on the sample with the p-type substrate. Filled circles represent holes and open circles represent vacant trap levels. The trapped charges between the green dotted line appear as the difference in the hysteresis width in Fig. 3 ($\Delta V_{L1} - \Delta V_{L2}$).
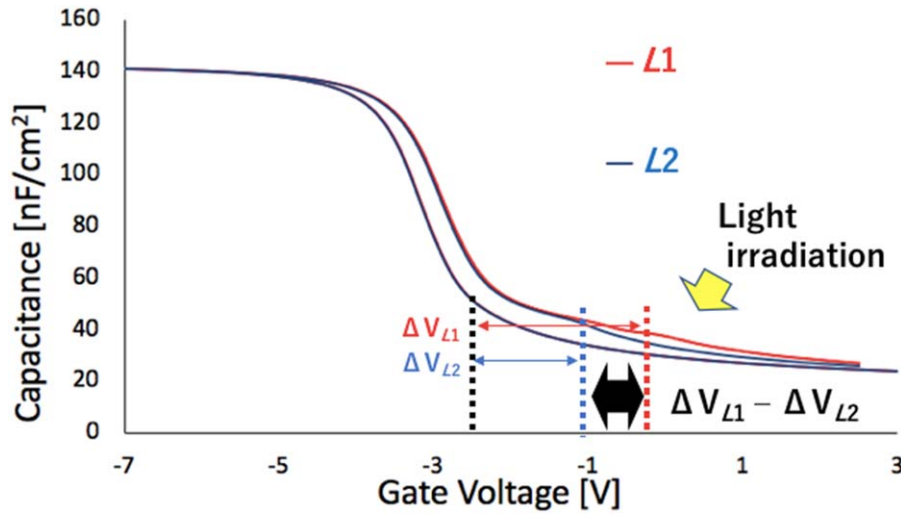
Fig. 3. (Color online) Typical example of photo-assisted C–V characteristics with two kinds of light wavelengths, $L1$ and $L2$. (Reproduced from Ref. 10).

the case of p-type substrates. For this case, the trapped charges will be excited when their energy levels referred to as the valence band edge (E_V) are less than the energy of light, while the energy levels should be referred to as the conduction band edge (E_C) for n-type. Note that this study uses only the light with photon energy well below the bandgap energy in contrast to the conventional photo-assisted C–V measurements where UV light with the energy above the bandgap is employed. Figure 3 shows typical photo-assisted C–V curves obtained at different wavelengths, $L1$ and $L2$. The small plateau observed in C–V curves around the region of maximum hysteresis will be approximately corresponding to the surface potential where the Fermi level comes closer to the energy level with the high density of the traps. But we do not focus on this energy level to avoid the ambiguous discussion to determine such levels under the possible influences of light-induced excitation of carriers. In this study, the amount of de-trapped charges will be detected as the maximum hysteresis width (ΔV_{L1} and ΔV_{L2}, respectively) in the C–V curves of each wavelength.

With this method, we newly define the effective interface trap state density (D_{eff}) by Eq. (1), using the difference of the number of traps ($C_{\mathrm{ox}}\Delta V/qE$) observed at different light energies, where C_{ox} is the oxide capacitance, q is an elemental charge, and E is the light energy

$$D_{\mathrm{eff}} = \frac{C_{\mathrm{ox}}(\Delta V_{L1} - \Delta V_{L2})}{q(E_{L1} - E_{L2})}. \tag{1}$$

Note that D_{eff} gives the total effective density of trapping states for a unit area, including not only the deep interface traps located on the surface of the semiconductor but the NITs located in oxide $\sim$Å or $\sim$nm away from the MOS interface. Note that the oxide traps located further than $\sim$nm are not taken into account as NIT in this study due to the very long time constant, which will be discussed later. Therefore, the traps with a wide variety of time constant are detectable by this measurement, except for very slow traps with a time constant longer than the sweeping time of C–V measurement (100 s, in our experiments).

Here it is worth mentioning how we can excite the trapped electrons in the region covered by gate electrode, even though we employ a nontransparent Au as the gate material.

To consider the light delivery to the region covered by the gate, we should remind that the absorption coefficient of SiC for visible light is so small that the light can penetrate the whole substrate easily. If we have a back contact electrode, we expect a sufficient intensity of visible light reflection on the backside. This reflected light can reach even the area covered by a gate. Actually, we confirmed that the electrode size of 1.5×10^{-4} cm^2 as small enough to excite the carriers under depletion bias by $\sim$1.8 eV UV light to observe the achievement of the inversion state using the same monochromator setup, while the electrode size beyond 3.0×10^{-4} cm^2 results in smaller response. Thus, the electrode size $\sim$5 × 10^{-5} cm^2 in this study is considered to be small enough to excite the trapped carriers in the oxide sufficiently under depletion bias. The validity of our experimental set up in terms of light intensity and irradiation time was also examined. From the light intensity dependence of hysteresis width with some of the wavelengths employed in the experiment, the hysteresis width was found to saturate when the light intensity was above 50% of the maximum intensity of the system. So, the maximum light intensity of the system in this experiment was confirmed to be sufficient to discuss the density of the trapped charges quantitatively. The appropriate light irradiation duration was also examined by observing the saturation behavior in the hysteresis width in the C–V curves. In our measurement, the irradiation time was set to 3 min because the hysteresis width was almost saturated by the irradiation for 3 min or more which was confirmed for some typical wavelengths.

3.2. Results of photo-assisted *C–V* with various wavelengths of light

In Fig. 4, D_{eff} determined from photo-assisted C–V measurements using Eq. (1) at 300 K are shown for both samples on p-type and n-type substrates, together with the energy distribution of D_{it} estimated by the high–low method using 1 MHz and 1 kHz. Without light irradiation, the hysteresis width of C–V curves was below 0.1 V. Both wet-POA and NO-POA improved the interface quality in terms of D_{it}, to achieve a similar $D_{\mathrm{it}} \sim 10^{11}$ cm^{-2} eV^{-1} at 0.2−0.5 eV from the conduction band edge (for n-type substrate samples) or the valence band edge (for p-type substrate samples). Even with a similar D_{it}, the difference in interface quality between
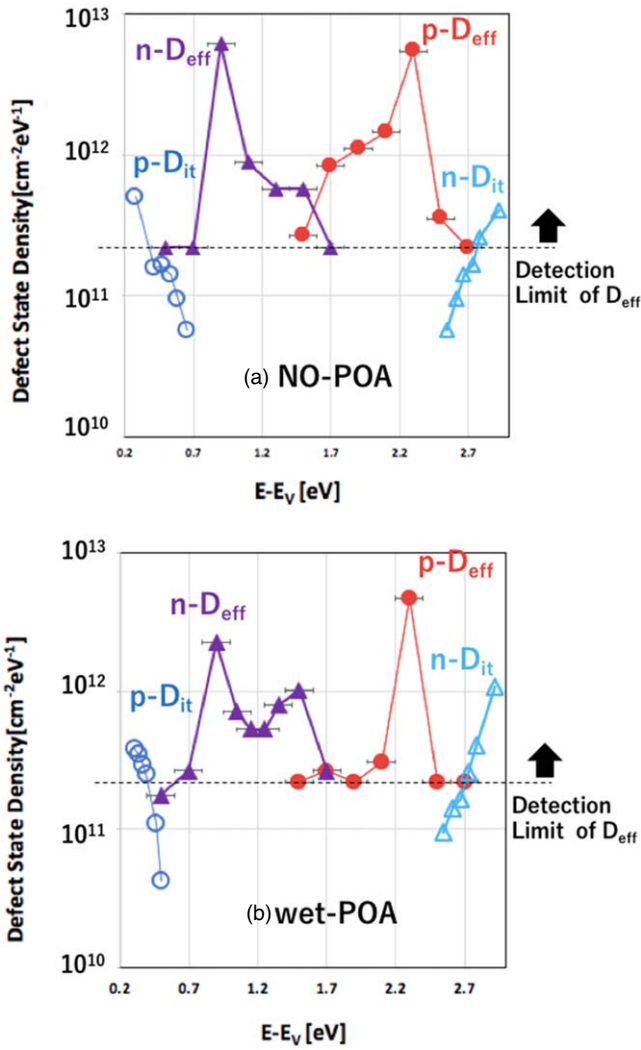
Fig. 4. (Color online) Energy distribution of D_{eff} measured at room temperature (RT; 300 K), for the samples with (a) NO-POA and (b) wet-POA. The distribution of D_{it} is also shown.

those samples with different POA treatments was clearly revealed by photo-assisted $C-V$ measurements at room temperature. From D_{eff} profiles, it can be seen that both samples showed effective trap state densities of $10^{12}-10^{13}$ cm^{-2} eV^{-1} for energy levels from 0.8 to 2.2 eV referred to E_V, However, near midgap state from 1.5 to 2.2 eV referred to E_v, the sample with NO-POA showed a broad energy profile whereas those trap state densities are almost suppressed (less than the detection limit of D_{eff}) for the sample with wet-POA. Instead, in the region of 1.5 eV, a small peak of D_{eff} was detected. It can be the characteristic trap of the wet-POA.

Next, we would like to discuss the possible origins of such deep traps revealed in this study by considering several candidate defect structures though we cannot determine which is the most probable one only from our experimental results. Simulation studies have been made on the expected energy levels of possible deep traps formed near the SiO$_2$/SiC interface with various origins.[24–27] As for the origins of the deep traps on the valence band side (0.7−1.6 eV referred to E_v), Si–CO–CO$_2$ (0.7 eV), (C$_2$)$_{Si}$ (0.9 eV and 1.5 eV), Si–(CO)–CO$_2$ (0.8 eV) and (C$_i$)$_C$ (0.8 eV) may be the candidates considering its suggested energy levels. On the

other hand, the possible candidates of the origin of the deep traps on the conduction band side (1.6−2.3 eV referred to E_v) would be Si$_3$–C (2.2 eV), C$_6$-ring (2.2 eV), Si–O–O–Si (2.3 eV) and (C$_i$)$_C$ (1.7 eV). Since the enhancement of the removal of CO from the SiO$_2$/SiC interface by H$_2$O[28] is expected for wet-POA, the significant reduction of near midgap states by wet-POA may be related to such structures consisting of C and O atoms. Especially in the region of 1.5 −2.2 eV, some of the deep states were reduced efficiently by wet-POA, though we cannot specify the most probable defect structure corresponding to that energy region only from our experimental data. Note that all of these candidate defect structures are carbon-related or carbonyl-induced defects and are characteristically present at the SiC MOS interfaces.

4. Photo-assisted $C-V$ characterized at various temperatures

4.1. Principle of photo-assisted CV characterized at various temperatures

Hysteresis measurements, like photo-assisted $C-V$ measurements, are the effective way to evaluate the NITs as we have discussed so far. However, a major restriction of the hysteresis measurement is the fact that the traps with a longer time constant than the voltage-sweeping time of $C-V$ measurement cannot be detected. Note that the time constant of charge trapping (τ) in NITs is generally approximated to be proportional to Fermi–Dirac function, which is given by Eq. (2) as an exponential function of measurement temperature, when we assume that the tunneling process in oxide from the interface to the trap is the rate-determining step of the carrier trapping process.[29,30]

$$\tau(\chi, T) = F(E, T)\tau_0(E)\exp(2\kappa\chi), \qquad (2)$$

where T is the measurement temperature and τ_0 is the time constant of the interface traps which weakly depends on T. χ is the tunneling distance of the traps. The notation κ is the tunneling attenuation factor for an electron wave function of energy E, which is a function of the tunneling mass of electrons (m^*).[31] F defines the ratio of available sites working as a receptor of tunneling electrons. The factor $\exp(2\kappa\chi)$ expresses the attenuation of tunneling probability for a given tunneling distance. It should be noted that the τ of de-trapping is strongly dependent on T because of the temperature dependence of F. For example, the estimated τ at 173 K becomes a few orders larger than that of 300 K. Here we assume as the effective mass, 0.30 m_0 for electrons and 0.58 m_0 for holes, respectively,[32,33] where m_0 is the mass of the free electron. As for the band offset, $E_C^{ox} - E_C^{SiC}$ at the SiC/SiO$_2$ interface was set to 2.7 eV where E_C^{ox} is the conduction band edge of oxide and E_C^{SiC} is that of SiC.[34,35] Using the above assumptions and mathematical relationships given in the literature, $\tau_0(E)$ and κ were approximately estimated. As a result, the temperature dependence of the approximate time constant of the traps with different distance from the interface were calculated[34] as shown in Fig. 5. Since our photo-assisted $C-V$ measurements were conducted with the voltage sweep rate ∼100 mV s^{-1}, we can roughly estimate the detection range of the location of the oxide traps from the relationship in Fig. 5. Note that the measurements at lower temperature will detect only the spatially shallower (closer to semiconductor) oxide traps
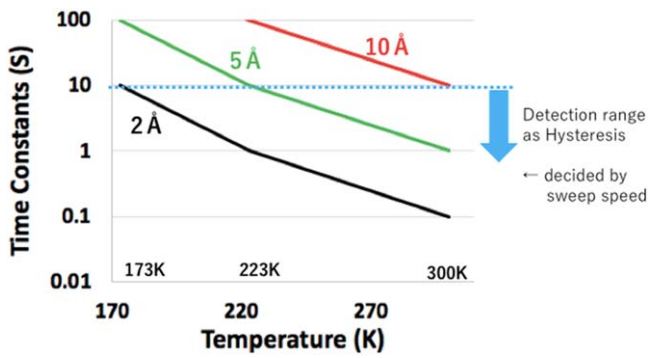
Fig. 5. (Color online) Estimated temperature dependence of the approximate time constants τ of the oxide traps with the different distances from the interface for the case of hole-trapping.

Fig. 7. (Color online) Energy distribution of D_{eff} at low temperature (223 K and 173 K) together with that at room temperature for the samples with (a) NO-POA and (b) wet-POA.

than those at room temperature, as illustrated in Fig. 6 for the case of hole-trapping. Thus, the photo-assisted C–V measurements at various temperatures can reveal the approximate depth profile of NITs.

4.2. Results of photo-assisted C–V characterized at various temperatures

The D_{eff} profile observed at lower temperatures (223 K and 173 K) on both p-type and n-type substrate samples is shown in Fig. 7 for the cases of (a) NO-POA and (b) wet-POA, respectively. As mentioned above, those low-temperature data are indicating the oxide trap density located closer to MOS interfaces than the ones observed at room temperature. From the figure, it is found that the effective trap state density in the region closer to the interface (173 K) seems to be a few times smaller than the one detected in the wider region (300 K) for the samples with NO-POA for the whole energy levels. On the other hand, for the sample of wet-POA, those in the region closer to the interface (173 K) is much smaller than those for the sample with NO-POA. It may seem strange that D_{eff} observed at 300 K for the energy range from 0.5 to 2.5 eV is smaller than that at lower temperatures. This is considered to be originated from a significant estimation error in the low temperature data, because of the coarseness of D_{eff} determination due to the large wavelength interval for low temperature measurements, as mentioned in Sect. 2. This
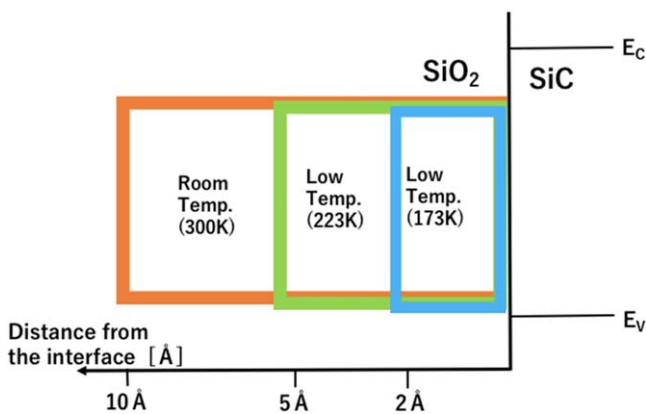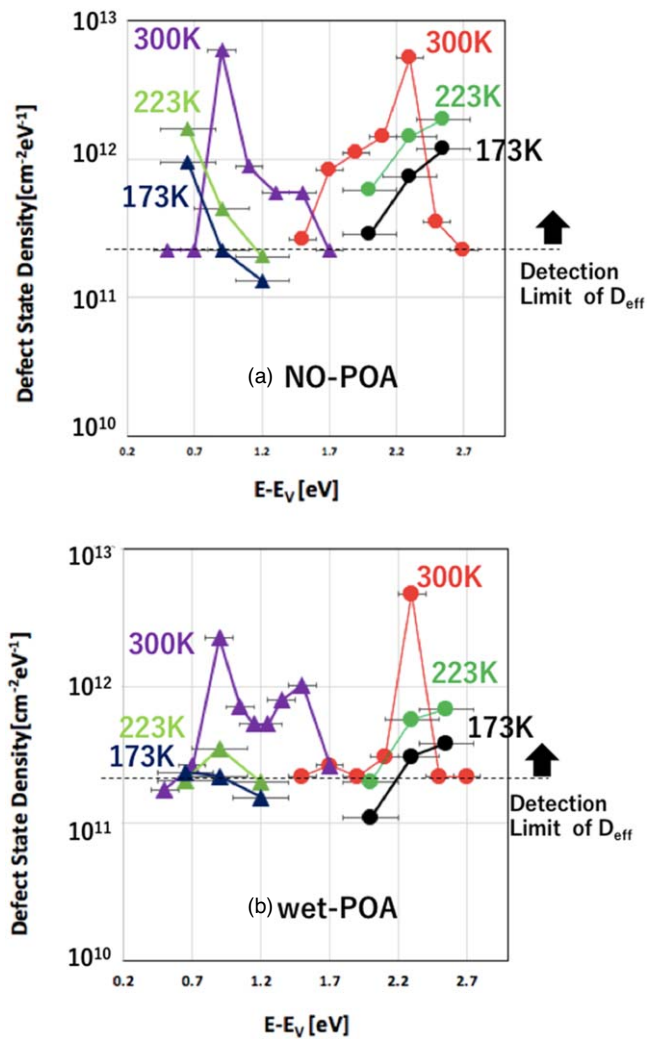
experimental condition difference between the room temperature (0.2 eV interval) and the low temperature (0.4 eV interval) measurements is caused by our experimental facility limitation.

Considering the quantitative relationship between τ and the distance of the traps from the interface shown in Fig. 5, the detectable distance at 173 K by $\sim$100 mV s^{-1} voltage sweep measurement was roughly estimated to be around half of that at 300 K as shown in Fig. 6. From D_{eff} profiles observed at lower temperatures, it can be seen that the sample with NO-POA showed higher effective trap state densities for whole energy levels than wet-POA sample. Our results would be reasonable if we assume an almost uniform spatial distribution of D_{eff} for NO-POA sample in the region within $\sim$1 nm distance from the MOS interface. On the other hand, D_{eff} detected at 173 K for the sample with wet-POA is as small as the level of D_{it}, which means that wet-POA suppresses the oxide traps in the region within several Å from the MOS interface quite more efficiently than NO-POA for the whole energy levels. This can be consistent with the fact that the field-effect mobility in both NMOSFET and PMOSFET fabricated with optimized wet-POA on (0001) substrates is a little better than that fabricated with NO-POA.[17,19]

Fig. 6. (Color online) Schematic of oxide trap detection range of spatial distance from SiO$_2$/SiC interface at different temperatures T, approximately estimated for the case of hole-trapping. The distance x of the trap states for τ < 100 s was roughly estimated, assuming the parameters such as tunneling attenuation factor κ. Here, trap level E was assumed to be close to the band edge.

5. Conclusions

In this study, we examined a characterization method of NITs with deep energy levels from two different viewpoints: the energy distribution and the spatial distribution of oxide traps. From photo-assisted C–V measurements with various wavelengths of lights at different temperatures, the difference in the deep trap profiles in the near-interface region of the SiC MOS interface fabricated by different processes was clearly revealed. For NO-POA, the trap levels uniformly exist both spatially and energetically, whereas for wet-POA, those are reduced more efficiently, especially in near midgap energy levels and in the spatial region of several Å from the MOS interface. Therefore, this method can be effective as a simple method for investigating the energy distribution and spatial distribution of oxide traps in the near interface region in wide bandgap semiconductor MOS stacks.

Acknowledgments

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